MULTILEVEL INTERCONNECT RELIABILITY

ON THE EFFECTS OF ELECTRO-THERMOMECHANICAL STRESSES

NGUYEN VAN HIEU

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Cover photo: SEM micrograph showing extrusion of Al through passivation layer.
Courtesy of John Vroemen from Philips Semiconductors Nijmegen.

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MULTILEVEL INTERCONNECT RELIABILITY

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DISSERTATION

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by

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born on April 16th, 1972
in Thua Thien Hue, Vietnam

This dissertation is approved by promoters:
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and assistant promoter
Dr. Ir. C. Salm

"Well done is better than well said"
Benjamin Franklin

In honor of my mother

To Phong Lam and Ha Trung,
… a very reliable wife and a wonderful son.

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Although this thesis has only one author's name, it has in fact been realized by many people. By writing acknowledgements one always runs the risk of forgetting somebody. To avoid this, I would like to start by thanking everybody who has in any way contributed to this thesis.

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Enschede, 14 February 2004

Nguyen Van Hieu

LIST OF PUBLICATIONS

Publications related to this thesis

This thesis is organized in six chapters and the four main chapters are built based on the publications listed bellow.

Chapters 2 and 3

[1] **Hieu V. Nguyen**, C. Salm, J. Vroemen, J. Voets, B. Krabbenborg, J. Bisschop, A.J. Mouthaan, F.G. Kuper, "Fast Thermal cycling stress and degradation in multiplayer interconnects", Proceedings of Semiconductor Advances for Future Electronics, 2001 (SAFE 2001), pp.136-140.

[2] **Hieu V. Nguyen**, C. Salm, J. Vroemen, J. Voets, B. Krabbenborg, J. Bisschop, A.J. Mouthaan, F.G. Kuper, "Test chip for detecting thin film cracking induced by fast temperature cycling and electromigration in multilevel interconnect systems", Proceedings of 9th International Symposium on the Physical and Failure Analysis of Integrated Circuits, 2002 (IPFA 2002), pp.135-139.

[3] **Hieu V. Nguyen**, C. Salm, J. Vroemen, J. Voets, B. Krabbenborg, J. Bisschop, A.J. Mouthaan, F.G. Kuper, "Fast temperature cycling stress-induced and electromigration-induced interlayer dielectric cracking failure in multilevel interconnection", Proceedings of Semiconductor Advances for Future Electronics, 2002 (SAFE 2002), pp.69-74.

[4] **Hieu V. Nguyen**, C. Salm, J. Vroemen, J. Voets, B. Krabbenborg, J. Bisschop, A.J. Mouthaan, F.G. Kuper, "Fast temperature cycling and electromigration induced thin film cracking in multilevel interconnection: experiments and modelling", Microelectronics Reliability, Vol. 42, 2002, pp. 1415-1420.

[5] **Hieu V. Nguyen**, C. Salm, B. Krabbenborg, J. Bisschop, A.J. Mouthaan, F.G. Kuper, "A reliability model for interlayer dielectrics cracking during very fast thermal cycling", to be published in the Proceedings of Advanced Metallization Conference 2003 (AMC 2003).

[6] **Hieu V. Nguyen**, C. Salm, B. Krabbenborg, J. Bisschop A.J. Mouthaan, F.G. Kuper, "Fast thermal cycling enhanced electromigration-induced extrusion failure in power IC metallization" Accepted for publication in IEEE Transactions on Devices and Materials Reliability (TDMR).

Chapter 4

[7] **Hieu V. Nguyen**, C. Salm, B. Krabbenborg, J. Bisschop A.J. Mouthaan, F.G. Kuper, "Electrothermomigration-induced failure in power IC metallization" Proceedings of Semiconductor Advances for Future Electronics, 2003 (SAFE 2003), pp.622-630.

[8] **Hieu V. Nguyen**, C. Salm, B. Krabbenborg, J. Bisschop A.J. Mouthaan, F.G. Kuper "Effect of thermal gradients on the electromigration lifetime in power electronics" to be published in the Proceedings of the International Reliability Physics Symposium, 2004 (IRPS 2004).

Chapter 5

[9] **Hieu V. Nguyen**, C. Salm, A.J. Mouthaan and F.G. Kuper, "Simulations of reservoir effect in multilevel Al-based metallization", Proceeding of Semiconductor Advances for Future Electronics, 2000 (SAFE 2000), pp.101-105.

[10] **Hieu V. Nguyen**, C. Salm, A.J. Mouthaan, F.G. Kuper, "Modelling of the reservoir effect on the electromigration lifetime", 8th Proceeding of International Symposium on the Physical and Failure Analysis of Integrated Circuits, 2001 (IFPA 2001), pp.169-173.

[11] **Hieu V. Nguyen**, C. Salm, R. Wenzel, A.J. Mouthaan, F.G. Kuper, "Simulation and experimental characterization of reservoir and via layout effects on the electromigration lifetime", Microelectronics Reliability, Vol. 42, 2002, pp.1421-1425.

Other publications

[12] **Hieu V. Nguyen**, N.D. Chien, "Modelling of metal oxide semiconductor field effect transistors (MOSFET)", Proceedings of the second National Conference on Solid State Physics, Vietnam, 1997.

[13] **Hieu V. Nguyen**, N.D. Chien, "Calculation of the threshold voltage of short channel MOSFETs based on the modelling of strong inversion and subthreshold region", Proceedings of the 7th National Radio-Electronics Conference, Vietnam, 1998.

[14] **Hieu V. Nguyen**, A.R Merticaru, R. Dekker, H. Kranenburg, A.J. Mouthaan, and N.D. Chien, "Formation of source and drain regions for a-Si: H TFT by using ion implantation through metal technique", Proceedings of Semiconductor Advances for Future Electronics, 1999 (SAFE1999), pp.123-127.

TABLE OF CONTENTS

CHAPTER 1

Multilevel Interconnects: Failures and Reliability

CONTENTS

Aggressive down scaling and the introduction of new materials for advanced interconnects can lead to several reliability concerns. This chapter briefly introduces electromigration and thermomechanical effects that underlie this work. First electromigration failures are discussed, including the basics of the electromigration phenomenon, different electromigration failure mechanisms such as voids open-circuit and extrusion short-circuit, and the effect of temperature gradients and thermomigration on electromigration. Second, thermomechanical failures due to thermal cycling are addressed, by introducing some basic mechanical concepts, deformation of metal films under thermal cycling, and thermal cycling as a reliability qualification test for microelectronic devices. Finally, the outline of this thesis is presented.

1.1 Introduction

Modern semiconductor chips include a dense array of narrow, thin-film metallic conductors that serve to transport current between the various devices on the chip. These metallic conductors are called interconnects as demonstrated in Figure 1.1. Interconnect reliability has been an important concern in the semiconductor electronics industry ever since the advent of integrated circuits (ICs). According to the technology effort to achieve denser, faster and more functional Very Large Scale Integrated (VLSI) circuits, the metal dimensions have shrunk and the interconnect system is becoming increasingly more complex. Shrunken metal lines may carry very high electrical current densities. These currents may lead to a transport of metal atoms due to "electron wind" that can result in permanent damages in metal lines by generating voids or hillocks at specific locations, this process is called electromigration. Electromigration is enhanced at an increased operating temperature. In Power IC's for example, multilevel interconnects may be subjected to large "on-off" electrical currents. Therefore, the combination of Joule heating and the heat dissipation from active devices cause interconnects to be subjected to very fast temperature swings as well as large thermal gradients. These stresses can induce thermomechanical failures due to the large differences in the material properties of the metal and the dielectric layers. Examples of these thermomechanical failures are cracking of a metal or a dielectric thin film and voiding.

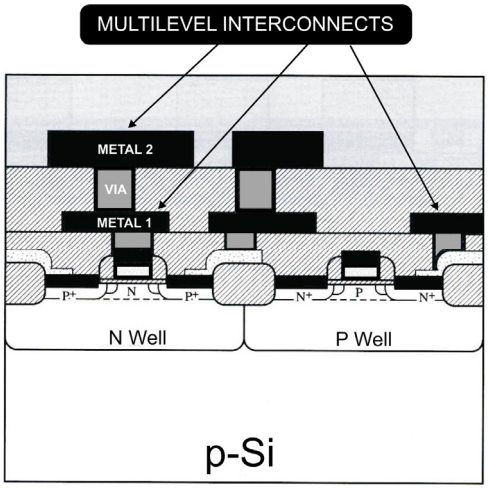


Figure 1.1. *A cross-section of a typical integrated circuit showing a multilevel interconnects.*

Otherwise, thermal cycling and thermal gradients can also lead to stressmigration and thermomigration, the movement of mass due to a stress or temperature gradient. Interestingly, fast thermal cycling and temperature gradients also seriously affect the electromigration performance as will be presented in Chapters 3 and 4. Therefore, these thermomechanical effects should be taken into account in the electromigration design rules during the design phase to improve the reliability of interconnect systems as well as of the final products. The study and understanding of physical failure mechanisms of these failures and their interactions are an extremely important aspect in IC reliability. Much research has been done to gain a fundamental understanding of electromigration and thermomechanical failures in multilevel interconnects, but a complete understanding has not been obtained yet. For example, the effect of temperature swings on the interconnect reliability is traditionally studied by means of temperature cycling in environmental chambers. The timeframe of the temperature cycles is much larger than in typical applications. Very fast thermal cycling mimics the operating conditions much closer, but its effect on the electromigration reliability has hardly been reported in literature. Similarly, the effects of temperature gradients within the chip have not received much attention.

This thesis will focus on electromigration and thermomechanical failures of Al-based interconnect that are currently used in many microelectronic products. The outline of the study presented in this thesis will be presented in more detail the end of this chapter. Recently, improved performance of interconnects was reported by switching from Al/SiO_2 to Cu/low-k interconnects [1]. This has reduced electromigration but also introduced new failure mechanisms [2]. For possible future applications carbon nanotube interconnects are being researched [3]. In this work the focus is on the reliability of the $AlCuSi/SiO_2(Si_3N_4)$ interconnect system. But as we will see in chapter 2, the observed failure, cracking of interlayer dielectric, also has potentially significant implications for advanced Cu/low-k dielectric interconnects.

In this chapter, some fundamental background knowledge related to the research in this thesis is given. The fundamentals of electromigration and thermomechanical failures will be presented in sections 1.2.1 and 1.2.2 respectively. Current reliability problems in multilevel interconnects that motivated this research will be also discussed in following sections.

1.2 Interconnect reliability concerns

Various failure mechanisms in multilevel interconnects should be concerned for a complete picture on metallization failures. However, the following sections will focus on electromigration and thermomechanical failures, including some basic concepts of importance to this thesis.

1.2.1 Electromigration-induced failures

The most common failures in metallic interconnects are related to electromigration, which is the mass transport of a metal due to the momentum transfer between conducting electrons and metal atoms. Electromigration causes failures in microelectronic devices by inducing voids, which eventually cause open circuits, or by inducing hillocks (extrusions), which can cause short circuits depending on the metallization geometry and the proximity of metal lines to one another. In the simplest case, void formation is strongly dependent on current direction. Voids will appear near the cathode, while hillocks may be found near the anode. As device features reduce in Ultra-Large-Scale Integrated (ULSI) circuits, current densities increase with the metallization layer complexity. These issues make understanding electromigration induced failure essential to design circuits that are more reliable.

Basic electromigration characteristics

When an electrical current passes through a conductor as shown in Figure 1.2, an atom flux J_{atom} is induced by the driving force due to the momentum transfer that can be calculated in the absence of other driving forces as follows [4];

$$J_{atom} = \frac{DC}{kT} z^* e \rho j \tag{1.1}$$

Where, D is the thermally activated diffusion coefficient ($D=D_o\exp[-E_a/kT]$), C is the concentration of diffusing atoms, kT is the average thermal energy, z^* is the effective charge, e is the electronic charge, ρ is the resistivity, j is the current density. Some of these factors come back when calculating the electromigration lifetime in terms of a mean time to failure (MTF) by the empirical equation, which was proposed by Black [5]. This so-called Black equation is expressed as:

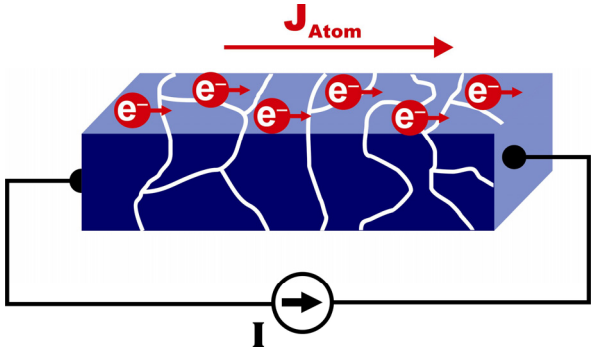


Figure 1.2. *A conductor under electrical current stress that causes the diffusion of metal atoms.*

$$MTF = Aj^{-n} \exp\left(\frac{E_a}{kT}\right) \tag{1.2}$$

Where, n and A are material constants, and E_a is the activation energy for electromigration. It can be seen that the electromigration kinetics follows an Arrhenius relation and is dependent on both temperature T and current density j. The use of Black's equation to predict electromigration-induced failure in a given system requires determination of both the activation energy for electromigration E_a and the exponent on the current density term n. Knowledge of these important parameters allows substitution of the actual use conditions back into equation (1.2) in order to obtain a reliable prediction of the expected mean time to failure (MTF).

A lognormal probability density function for the time-to-failure is generally used

$$f(t) = \frac{1}{\sigma t\sqrt{2\pi}} \exp\left[-\frac{1}{2}\left(\frac{\ln(t/MTF)}{\sigma}\right)^2\right], \; t \geq 0 \tag{1.3}$$

Where, f(t) is the probability of the failure time, t is the lifetime expressed as a continuous variable (the time-to-failure) and σ is the lognormal standard deviation.

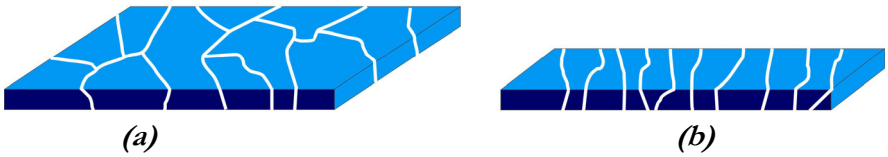
Effect of microstructure on electromigration

It has been well known for a long time that electromigration performance is significantly correlated to the microstructure of the metal line. The effect of the microstructure on the electromigration lifetime has been extensively

studied. Metal atoms diffuse much faster along a grain boundary or an interface than through the bulk material. The corresponding activation energies for electromigration, as reported in literature are presented in Table 1.1 [6]. From equation (1.2), it is clear that the diffusion along grain boundaries plays more important role in line failure than the diffusion through the bulk of the metal. Interestingly, the median electromigration lifetime decreases as the line width and thickness decrease, but when the linewidth becomes comparable with the grain size, the electromigration lifetime increases. An early study by Vaidya and et. all reported that the lifetime decreases as the line width is reduced from 4μm to 2μm, and when the line width is reduced to a smaller than 1μm, the lifetime increases [7]. A well-accepted explanation is that there is a change in microstructure from grain columnar to grain bamboo structures when reducing the linewidth to a comparable size with grain size as depicted in Figure 1.3. In the columnar grain structure, there is grain boundary pathway in the direction of electric current. In the bamboo grain structure, grains span entire the width of the metal line, and are more or less perpendicular to the electric current and act like diffusion barriers. Therefore, several factors are attributed to the improvement of the electromigration lifetime of the metal line with bamboo grain structure as follows; (i) the number of grain boundary pathways for diffusion along the metal line is small, thus the amount of mass transport is less; (ii) as the number of grain-boundary triple points per unit length is reduced, so is the number of divergence sites for atom flux;

Table 1.1*. Observed activation energies for electromigration [6].*

Materials	**E_a [eV]**		
	Bulk	Grain boundary	Surface
Al	1.4	0.4-0.5	–
Al/Cu	1.2	0.6-0.7	0.8-1.0
Cu	1.3	1.2	0.7-1.0



(a) ***(b)***

Figure 1.3. *Different microstructures in metal line; (a) near-bamboo grain structure; (b) bamboo grain structure.*

(iii) the electromigration flux is reduced since most of the grain are perpendicular to the direction of current flow.

Electromigration-induced voids

Void formation was first identified as a failure mode by Black [8] over 30 years ago. Voids (see Figure 1.4) can grow and link together to cause electrical discontinuity in conductor lines, which leads to open-circuit failure. Several models to describe this failure mode have been proposed in literature. However, one model, based on the opposing driving forces of electromigration and concentration gradient agrees well with the experimental observations [9]. This model argues that as atoms migrate in a conductor, local changes in mechanical stress occur. Compressive stresses where the metal atoms accumulate and tensile stresses appear where the metal atoms deplete. As a result, mechanical stress gradient are formed within a conductor undergoing electromigration, which generates a flux of atoms to oppose the electromigration flux. The flux is now given by [10,11]:

$$J_{atom} = \frac{CD}{kT}\left(z^{*} ej\rho + \Omega \frac{\partial \sigma}{\partial x} \right) \tag{1.4}$$

Where, $\partial\sigma/\partial x$ is the stress gradient and Ω is the atomic volume. In the ideal case of a structurally uniform conductor with no temperature gradient, there is no flux divergence so that electromigration-induced damages will not occur. Most conductors used in interconnects are polycrystalline thin films containing structural defects.

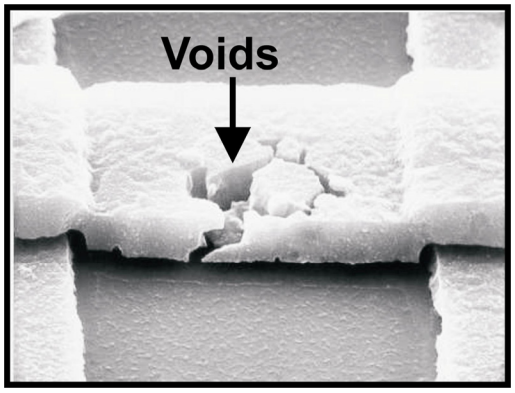


Figure 1.4. *Scanning electron microscope images of electromigration-induced voids in aluminum interconnects.*

This means that there are always divergences of atom flux existing at places where the number of atoms flowing into the area is not equal to the number of atoms flowing out. Consequently, damages are induced at points showing a change in atom concentration. Voids occur in the areas where atom mass transport results in mass depletion.

On the other hand, whisker and hillocks are formed in the areas of mass accumulation, and they can result in an extrusion failure mode. Electromigration-induced void formations have been extensively studied in Al-base metallization [12-14].

Recently, this failure mode has also received much attention in Cu-base metallization. A thorough review of literature however [15], indicates that activation energies for electromigration in Cu are strongly dependent on process variations, so while the "good" Cu metallization systems will show activation energies over 1eV, these can also be 0.6eV and lower, which is actually worse than in state of the art Al:Cu metallization [16]. Actually, electromigration-induced void formations at via bottom interface are serious reliability concerns in Cu multilevel interconnects, and it has been extensively studied in the past few years [16-18]. Also, stress-induced voiding at the via is also an important issue that has been recently investigated [10,19,21]. This failure mechanism could be suppressed through technology and design optimizations when it is fully understood.

Electromigration-induced extrusions

As mentioned above, electromigration can also induce extrusions where there is an accumulation of metal atoms, resulting short-circuit or cracking of dielectric failures. There is a general belief that void-induced open circuit failures usually appear at an earlier time than extrusion-induced short-circuit in Al-based metallization [4]. However this might not be true for very complex modern VLSI chips with around an order of million conductor lines per chip and the spaces between the conducting lines dramatically decreases. In an early study about the relation between short-circuit and open-circuit induced by electromigration, Lloyd showed that both failure mechanisms can be mixed and treated as part of the same failure mechanism in multi-layer VLSI [22]. Other studies by Tower and co-workers [23-25] have shown influences of the dielectric (passivation) thickness and material properties of

dielectrics and Al-alloy metallization on the electromigration-induced extrusion that results in a short circuit.

Recently, there is a desire to implement low-k dielectric materials in advanced interconnects, which have poor thermomechanical properties. Electromigration-induced extrusion short circuit and cracking of interlayer dielectric failures as demonstrated in Figure 1.5 can become more important issue [26,27]. Electromigration studies in Cu have progressed rapidly since it has been identified as the metallization system that will be replacing Al metallization in future microelectronic circuits. However, electromigration-induced extrusion failure was reported to be still a problem in Cu interconnects [28]. It is recently reported that the extrusion failure mode in wide and narrow Cu lines has a shorter extrapolated the lifetime than voiding [29]. The transition to Cu as the interconnect material of choice is accompanied by the introduction of low-k dielectrics, which are more compliant and have lower fracture toughness [30] compared to conventional dielectrics such as Si_3N_4 or SiO_2. The fact that the former property may reduce the back-stress force and the latter property makes the dielectrics susceptible to cracking due to compressive stress induced by electromigration. Electromigration with the extrusion failure mode related to the fracture toughness of dielectrics has recently been reported in the literature [27,31]. It was shown that low fracture resistance dielectrics are more susceptible to crack by electromigration driving forces.

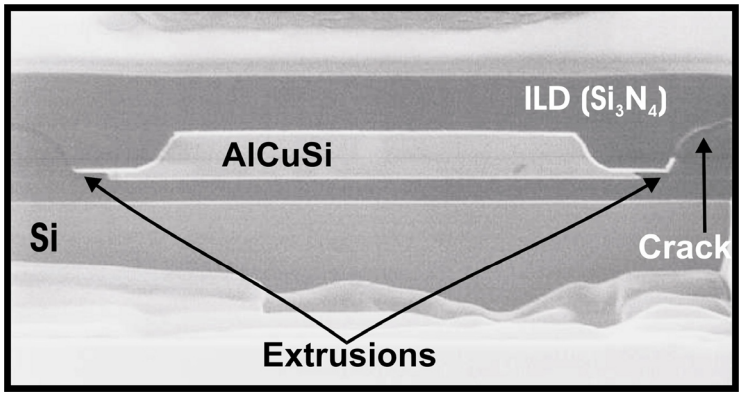


Figure 1.5. *Scanning electron microscope images of electromigration-induced extrusion and cracking of interlayer dielectrics in AlCuSi metallization.*

Both issues (faster interfacial/surface diffusion of copper and poor mechanical properties of low-k dielectric) could cause the electromigration-induced extrusion to become a serious problem in Cu interconnects.

Electromigration in multilevel interconnection

In multilevel interconnects, there are numerous contacts connecting the metal line from one level to an adjacent level to a semiconductor junction or to a metal line (see Figure 1.1). The electromigration behaviour at these contacts is usually very different from those of the metal line. W-plug vias are usually used in conventional Al-based multilevel interconnects. The W-plug acts as a blocking boundary for electromigration. Since no Al can pass through this blocking boundary the migration of atoms will cause an accumulation of material at the upstream of the line and a depletion of material at the downstream end of the line. This flux divergence at the W-plug site would suggest that the via is the weakest link in multilevel interconnects, and it can be the cause of a shorter electromigration lifetime in multilevel interconnects compare to single layer, as demonstrated in Figure 1.6 [32]. This failure mechanism has been extensively studied so far [32,33].

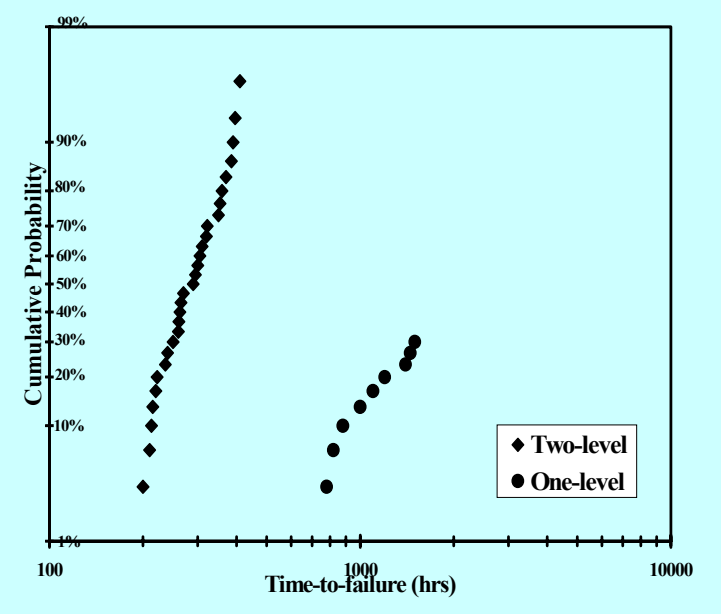


Figure 1.6. *A comparison electromigration reliability of two (line segments connected by W-plugs) and single level interconnects under the same stress condition [32].*

Although Cu-based multilevel interconnects do not have W-plugs, electromigration-induced voiding at the via is still a reliability concern [34]. Therefore, there is a great interest in the semiconductor industry to better understand the physics/materials science of the via electromigration failure to further fuel technology development progress.

Effect of temperature gradient and thermomigration

As mentioned above, electromigration only induces damages when there are divergences of atom flux. When this phenomenon is used in a physical model, it can be known that the change in the metal atom concentration at a point due to the flux divergences must be in accordance with the mass continuity equation [35], expressed as:

$$\frac{\partial C}{\partial t} = -\nabla \cdot J \tag{1.5}$$

Where C is the atomic concentration. From equation (1.5), we can see that in case $\nabla \cdot J=0$ (no flux divergence), as much material would reach any section on the metal line, as is leaving that same section, and no damage is induced by electromigration. If on the contrary, $\nabla.J\neq 0$ (flux divergence), there will be damages-induced; $\partial C/\partial t<0$, mass depletion occurs and voids form; $\partial C/\partial t>0$ mass accumulates and hillocks form.

When a metal line is subjected to a temperature gradient, an additional force exits. The temperature gradient can exist both globally or locally in the metal line due to heat generation from Joule heating or power dissipation from active devices on the chip as illustrated in Figure 1.7. Under a driving force of electron flow, atoms move from cathode to anode. At the hottest region of the metal line, atoms accelerate and move ever faster because of the strong thermal activation of the ion mobility. Therefore, on the cathode site of the hottest region, atoms move out faster than they move in, resulting in mass-depletion and void formation. The reverse happens on the anode site of hottest region, where atoms move in faster than out, resulting in mass-accumulation and hillock formation (see Figure 1.7). Generally, for electromigration in the presence of a temperature gradient, void formation occurs in the regions where electron flow is in the direction of increasing of temperature, and hillocks form in the location where electron flow is in the direction of decreasing temperature.

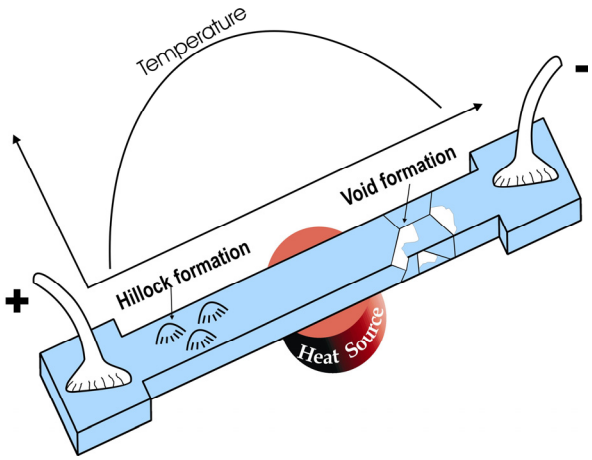


Figure 1.7. *A metal line under heat generation from dissipation of active devices.*

It is clear that temperature gradients are important sources of atomic flux divergence, since the flux depends exponentially on temperature (see Equation 1.1). Therefore, in the presence of a temperature gradient, electromigration induces damage not only due to flux divergence at grain boundary (blocking boundary) but also due to flux divergence by temperature gradient, and hence there is a competition between two failure mechanisms. The relation between the two failure mechanisms has been extensively studied in [36]. Temperature gradients can also lead to thermomigration, although mass migration due to temperature gradient is usually small compared to electromigration for Al metal lines. The total atomic flux as expressed in equation (1.4) must be extended with the thermomigration-driving force, and it becomes [37]:

$$J_{atom} = \frac{CD}{kT}\left(z^{*} ej\rho + \Omega \frac{\partial \sigma}{\partial x} + \frac{Q^{*}}{T}\frac{\partial T}{\partial x} \right) \tag{1.6}$$

Where, Q* is the heat of transport, and (∂T/∂x) is the temperature gradient. Recently, Ru [38] has theoretically reported that thermomigration is the leading driving force for instability of the electromigration-induced mass transport in interconnect lines, and it plays a significant role in the EM failure of interconnect lines.

The scaling in microelectronics drives the metal line dimension to smaller and smaller sizes, and they are surrounded with low-k dielectric materials, which are poor thermal conductors [30]. This could result in a noticeable

temperature gradient in the metal line due to the Joule heating and power dissipation from active devices. This condition can enhance electromigration and induce thermomigration phenomena, accordingly. Therefore, there is a need for better understanding of these phenomena with hope to minimize this effect by introducing new manufacturing processes and/or design schemes.

1.2.2 Thermomechanical failures

Thermomechanical failures arise from thermal cycling. Large stresses can develop in thin metallic films (interconnects) attached to the semiconductor because of the large difference in thermal expansion coefficients between metals and dielectrics or semiconductors in microelectronic devices. These thermal cycles can occur during thermal excursions encountered in processing steps or during operation. These thermal stresses may induce plastic deformation of the thin films accompanied by creep and interfacial sliding, and have a pronounced effect on the interconnect reliability.

Thermally cycled Al thin films have been extensively studied in literature and different failure mechanisms have been reported [39,40]. Other experiments revealed that following thermal cycling, Al films expanded relative to the Si substrate, whereas Cu films shrunk, resulting in an alteration of the film-footprint on the substrate in both cases [41]. The tendency of Cu to contract in volume and form intergranular voids due to surface diffusion is an additional reliability concern with respect to Cu interconnects that was not a major issue in the present Al interconnect technology [15,42]. Thermal cycling induced void formation can affect interconnect reliability, and also accelerate electromigration by an earlier void nucleation time. Early onset of void formation could seriously degrade with electromigration, causing larger voids and open circuits [43]. These expectations indicate that the reliability concerns, regarding to thermomechanical failure of advance interconnects still remains a concern in the future.

Mechanical material behavior: elasticity and plasticity

Mechanics play an increasingly important role in the reliability of electronic devices, where the complexity of integrated circuits is increasing rapidly. To understand the mechanical effects on their reliability, some basic mechanical concepts are shortly presented here. Diagrams as shown in Figure 1.8 are the

most common pictures of mechanical behavior of materials that are loaded in tensile state. When we apply a load to a specimen so that the stress and strain go from the origin O to A. At this point, when the load is removed (unload), the material returns to the original state (see Figure 1.8a). This property of a material is called elasticity. If we apply a higher level of the load to the same material the stress and strain will go from origin O to B, when it unloads, the material follows line BC on the diagram (see Figure 1.8b). At point C, the material is not loaded, but it gains a residual strain (permanent strain, represented by line OC). The strain OD as the material loads at point B, and the strain CD is called elastic recovery strain. Point E (see Figure 1.8a and b) between points A and B is defined as an elastic limit, below which the material is elastic beyond which the material is plastic. When a material undergoes a load in the elastic region, there is no significant change in the material properties after releasing the load. When a material undergoes a load in the plastic region, material properties change after releasing the load, and the permanent strain exists in the material. Now, we suppose that the material after the plastic deformation is reloaded. The new load begins at point C (see Figure 1.8c) and continues upward to point B, and then the material follows the stress-strain curve to point F.

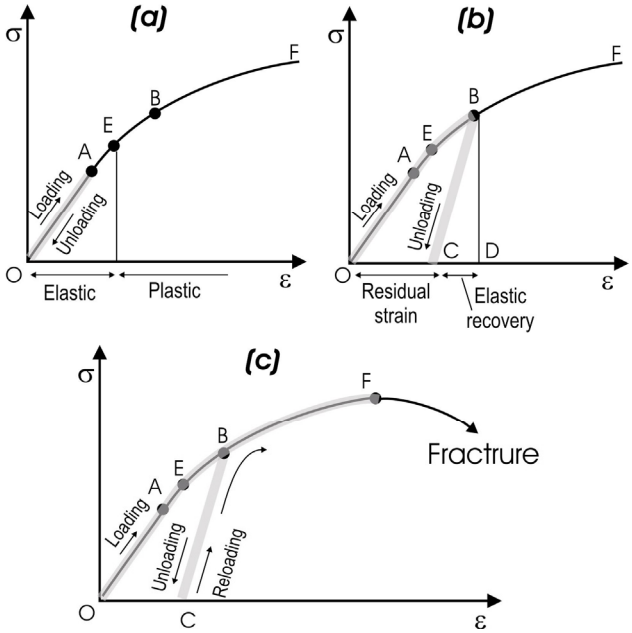


Figure 1.8. *Stress-strain diagrams of a metal: (a) elastic behavior, (b) plastic behavior, (c) reloading of a material.*

Thus, the second load can be imaged as similar as the first load but applied to a "new material", which has already a residual strain. The "new material" has a lower amount of yielding beyond the elastic limit (from B to F) compared to the origin material (from E to F). A repetitive load can bring material over the amount of yielding, and the material becomes "soft" before it is fractured. The maximum stress that material can support the load without any fractures is called the fracture stress (fracture strength). Brittle materials (e.g. SiO_2, Si_3N_4) have the same behavior but they behave linearly until their fracture stress.

Metal film deformation during thermal cycling

When a metal film deposited on a silicon substrate is subjected to temperature cycling with a temperature change of dT, the in-plain strain of the substrate changes by $\alpha_s dT$, where, α_s is the thermal expansion of the substrate. Since the film is bonded to the substrate, the in-plane strain increment of the films equals that the of substrate, namely [45],

$$d\varepsilon^p + d\varepsilon^e + \alpha_m dT = \alpha_s dT \tag{1.7}$$

where, ε^p and ε^e are the plastic and the elastic in-plain strain in the metal film. That is, the thermal expansion mismatch between the metal film and the substrate is accommodated by a combination of elastic and plastic strain in the metal film. The elastic in-plain strain of the film relates to the biaxial stress in the film by Hooke's law:

$$d\varepsilon^e = \frac{1-\nu_m}{E_m} d\sigma_m \tag{1.8}$$

Where E_m is the Young's modulus and ν_m is Poisson's ratio of the film. When the film is elastic, $d\varepsilon^p=0$, the thermal stress in the film can be calculated from equation (1.7) and (1.8) as follows:

$$d\sigma_m = -\frac{E_m}{1-\nu_m}(\alpha_m - \alpha_s)dT \tag{1.9}$$

Substituting equation (1.8) in equation (1.7) gives the increment of the plastic in-plane strain

$$d\varepsilon^p = -(\alpha_m - \alpha_s)dT - \frac{1-\nu_m}{E_m} d\sigma_m \tag{1.10}$$

The in-plain strain of the metal during the temperature cycling can be calculated by integrating the equation (1.10). Note that the thermal expansion coefficient and Young's modulus are in general temperature dependent.

Thermal cycling as a qualification test

Microelectronic components or devices are typically made of different materials, including metals, ceramics, polymers. When they are subjected to a thermal cycling this can cause degradation or permanent damage. Thermal cycling has been extensively used as a qualification test for a long time [46]. Conventionally, after a thermal cycle test, a device is functionally tested, and if needed failure analysis is carried out in order to derive failure model. Different failure models of multilevel interconnects under thermal cycle tests have been observed for many years in the past that are typically: (i) crawling of the metal films [47,48]; (ii) cracking of passivation and interlayer dielectrics [50,51]. If the failure model is fully understood, one makes a new device by modifying either processing parameters or design or materials to avert the failure. Then the new device is tested again with thermal cycling to be sure that the modifications postpone the failure and not cause another failure. If the device passes a certain number of thermal cycles without failing, one pronounces that the device passed the qualification test. The iterations of qualification tests may take a long time to converge, because the modification to avert one failure mode can be possible cause another failure mode. Therefore, alternatives of test method to shorten testing time to quickly converge the qualification test can be of great importance.

1.3 Outline of this thesis

This thesis deals with multilevel metallization reliability of aluminum based power IC's. This chapter has presented typical failure models such as electromigration and thermomechanical failures, including the basic concepts that are related to the research in this thesis. In chapter 2, a fast thermal cycling method for interconnect reliability tests is studied, its application for investigating thermomechanical failures of a standard two level metallization interconnect is demonstrated in detail. Through the investigation, the failure mechanism is well understood, a reliability model for fast thermal cycling is developed, and the impact of dielectric materials on the failure mechanism is also treated. In chapter 3, the well-known electromigration failure that current

interconnects cannot yet avoid is addressed. Electromigration-induced extrusion failure is mainly dealt with, and influence of fast thermal cycling on the failure model is studied. Chapter 4 presents a study into electro-thermomigration of power ICs, for which special test chips have been designed to impose and measure the temperature gradient. In chapter 5, reliability improvement of multilevel interconnects by design layout is presented. Characterizations are done through simulations and experiments for comparison. Finally, chapter 6 summarizes the research work presented in this thesis, draws conclusions of this work, and offers suggestions for future work.

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CHAPTER 2

Fast Thermal Cycling-Induced Thin Film Cracking

CONTENTS

In this chapter, a fast thermal cycling test method for reliability tests on multilevel interconnects, without using an environmental chamber, is presented in detail. The test method is applied to study the reliability of a standard two level metallization currently used for power IC's. First, the fast thermal cycling tests were performed under different conditions. The failure rate is well represented by a Weibull distribution, and distribution parameters are generally similar for all test conditions. The Coffin-Manson equation can be used to express the failure rate with respect to number of cycles-to-failure as a function of the temperature cycle range, but only under certain test conditions. The exponent value in Coffin-Manson equation was found to be q=8.4, indicating a failure mechanism related to cracking of brittle materials. That was confirmed by failure analysis that revealed cracking of the interlayer dielectric as the cause of failure. Secondly, a model is developed to explain the observed failure mechanism. Then a reliability model has been developed to express the failure rate as a function of the temperature cycle range for all the test conditions of the fast thermal cycling test. Eventually, the difference between two interlayer dielectric materials (SiO_2 and Si_3N_4) on the multilevel interconnect reliability was investigated. The outcome of this comparison may have implications for advanced interconnect systems using low-k interlayer dielectric materials, as will be discussed.

2.1 Introduction

With increasing power dissipation and decreasing chip size, thermomechanical failures in multilevel interconnects are more likely to become a reliability problem. Multilevel interconnects are made of a stack of different materials such as metals, dielectrics, polymers, and semiconductors. These materials have dissimilar mechanical properties. Therefore, thermal cycle load is one of the main factors that generate stresses resulting in cracking of thin films due to the large thermal mismatch between metallic and dielectric materials and the silicon substrate. Thermal cycles are experienced during thermal excursions encountered in processing steps or during normal use. Therefore, these thermal cycles are impossible to avoid. These thermal stresses may induce plastic deformation of the thin films accompanied by creep and interfacial sliding, and have a pronounced effect on the reliability of multilevel interconnects. Predictions of thermal cycling failure rates for integrated circuits (ICs) have been widely discussed so far, because the thermal cycling test is extensively used in the microelectronic industry to qualify new products [1]. Recent publications have addressed issues of interconnect system failures due to thermal cycling. They have reported that the thermal cycling can crack metal films [2,3] as well as interlayer dielectrics [4,5], resulting in IC failures. In order to use this understanding to improve multilevel interconnect reliability, failure mechanisms must be understood well enough to create a good failure rate model. However, thermal cycling using an environmental chamber is far from the real operating condition of ICs, which work at high operating frequencies. Such "slow" thermal cycling test could mask failure mechanisms more relevant to the application fields and may actually prevent detection of failure mechanisms likely to occur in application environments. These imply that fast thermal cycling (FTC) test is more representative of the field use conditions. Another advantage of a FTC test is that the typical cycle time is orders of magnitude shorter than the conventional thermal cycling test. Therefore, the FTC test will enable quick reliability assessment and help in reducing development and cost. These issues are very important because the cost and the time-to-market are key for competing in global markets. Therefore, a FTC test could be an important accelerated test to qualify microelectronic products. However, up till now, a FTC test suitable for reliability testing of multilevel interconnects is still lacking. The aim of the work described in this chapter is to present a FTC test

method that can be used for the reliability test on multilevel interconnects. Firstly, the test method of FTC is demonstrated, including a description of the test chip design, process simulation of the test chip, a test set-up, and the development of a reliability test system. Secondly, the test method is applied to study the reliability of a standard two level metallization currently used in power ICs. The reliability test results, the failure analysis, and the modelling of the failure mechanism are discussed respectively. Following this, a reliability model will be presented. Finally, a study of the impact of interlayer dielectric materials on the multilevel interconnect reliability is presented.

2.2 Fast thermal cycling technique

The following sections will present important features that are required to perform the FTC test. All experimental data and calibration results of this section will be implemented in the section 2.3 and chapter 3.

2.2.1 Description of the test chip

Design of the test chip[6]

The test chip used to carry out the FTC test is designed with a number of important features as shown in Figure 2.1. There is a very large n^+-Si resistor (about 4Ω) just below the die surface, which acts as a micro-chuck, and there is an integrated p/n diode in the middle of the resistor, which acts as a temperature sensor. The micro-chuck is used to generate temperature swings and the temperature sensor is used to monitor them. The test chip has two metal layers. The metal 1 (M1) is a very long meandering line resistor, located on the die surface as a stressed line (SL). The total length, the width, and the thickness are 4000μm, 3.5μm, and 1μm, respectively. In between the meandering line, additional tracks on both sides are implemented in M1 to detect sideways short circuits. The spaces between the metal line and the tracks are 3.5μm. The metal 2 (M2) is a large plate over the whole structure to detect interlayer short circuits and its thickness is about 2.5μm. The space between M1 and M2 is 0.9μm (the thickness of the interlayer dielectric layer). The passivation and the interlayer dielectric (ILD) layers are silicon nitride deposited by PECVD (plasma enhanced chemical vapor deposition). The thickness of the passivation layer is 1.0μm. Additionally, the test chip has a standard electromigration test element but this will not be used in this study.

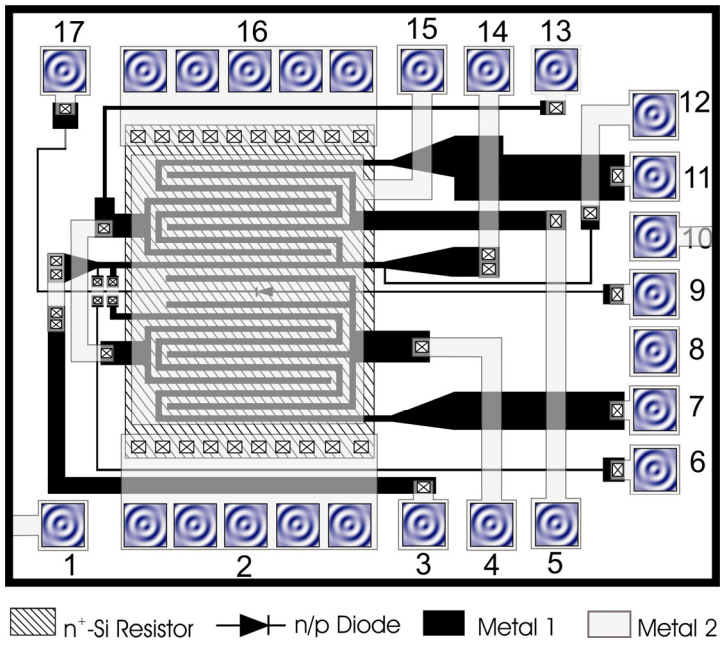


Figure 2.1. *The top view of test chip for the fast thermal cycling stress*

Table 2.1. *Function of the pins of test module*

Pin	Name	Function
1	S	Substrate connection, connect to lowest available voltage
2	I_R^-	Connection of the 4Ω power resistor
3	I_{EM}^-	Current connection for electromigration test
4	EXTR.	Extrusion monitor to M1
5	EXTR.	Extrusion monitor to M1
6	V_{EM}^-	Voltage connection for 4 point resistance measurement
7	V_{TOT}^-	Connection for M1 line for 2 point resistance measurement
8	n.c.	Not connected
9	C	Cathode of diode for temperature measurement
10	S	Substrate connection, connect to lowest available voltage
11	V_{TOT}^+	Connection for M1 line for 2 point resistance measurement
12	V_{EM}^+	Voltage connection for 4 point resistance measurement
13	EXTR.	Extrusion monitor to M 1
14	I_{EM}^+	Current connection for electromigration test
15	EXTR.	Extrusion monitor to M2
16	I_R^+	Connection of the 4Ω power resistor
17	A	Anode of diode for temperature measurement

The test chip is encapsulated in a standard 17 pins plastic package of power ICs to simulate the effects of real power ICs. The function of the 17 pins of the test chip is summarized on Table 2.1.

Process simulation of the test chip

To gain a better understanding of the effects of process, a model of the test chip is implemented in a commercially available process and device simulator (SILVACO). The simulation processing steps are copied from the technology processing steps. Figure 2.2 shows a cross-section of test structure by Focus-Ion-Beam (FIB) and the result of simulation structure. It can be seen that the geometry of process and simulation structures are quite comparable. The aim of the test structure is to investigate electro-thermal mechanical stresses. Therefore, the simulation structure is very useful because it can be used to estimate some important parameters such as residual stress after process, stress due to thermal expansion, and the temperature distribution. These will be implemented in next chapter to understand and explain the failure mechanism.

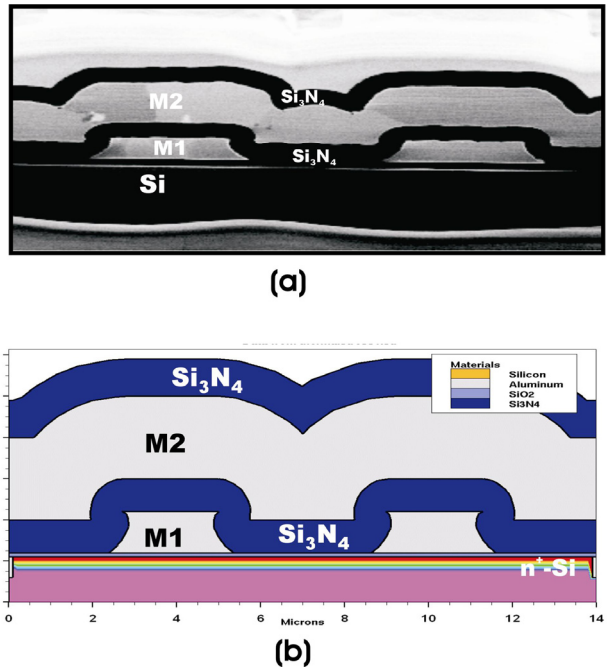


Figure 2.2. *The cross-section of the test structure; (a) is FIB image, (b) is the simulation structure.*

2.2.2 Description of the experimental set-up

To perform the reliability tests by the FTC stress with the test chip as described above, an experimental set-up must include some important functions such as the generating and monitoring fast temperature swings, detecting device failure and possibly carrying out the tests with a large number of devices. The following subsections will describe in detail the experimental set-up that was used for the reliability tests with the FTC stress.

The set-up for fast thermal cycling test

A diagram for the FTC set-up test is demonstrated in Figure 2.3. The set-up has three important blocks. Block (I) can be considered as a pulsed current source, which is used to force pulsed current through the n^+-Si resistor (micro-chuck) to generate temperature swings. This pulsed current source has an adjustable amplitude, frequency and duty cycle. Thus, different temperature swings (a range of T_{min}, T_{max}, and ΔT) can be achieved.

Block (II) is a scheme for measuring the temperature with the integrated diode temperature sensor. This scheme incorporates a current source (2) and a digital oscilloscope (3) to force a DC current through the diode and to monitor the variation of voltage across on the diode due to the temperature swings, respectively. When the temperature coefficient of the diode is known, the temperature swing profile can be translated from the diode voltage waveform (a variation of diode voltage by the change of temperature).

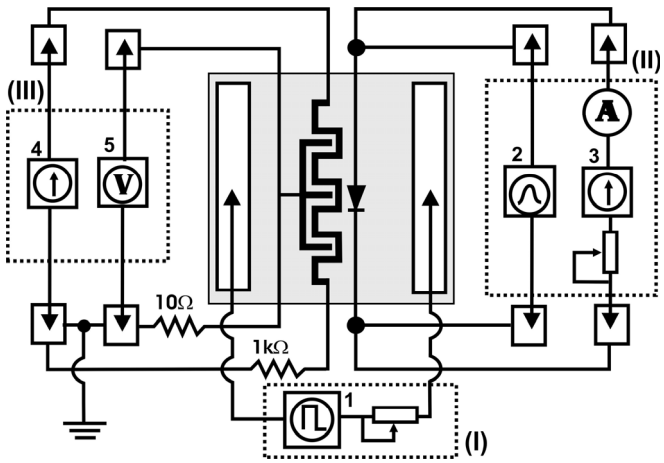


Figure 2.3. *The set-up for the FCT test: block (I) is the temperature generation scheme; block (II) is the temperature measurement scheme; block (III) is device failure detection scheme.*

Block (III) is a scheme to detect device failure. Depending on the test chips and test purposes, this scheme can be made appropriate to their situation. In this work, block (III) is used to detect short circuit failures, including the sideways (in M1) and the interlayer short circuits (between M 1 and M 2). As can be seen in Figure 2.3 (see block III), the stressed line (about 400Ω) is connected with a resistor (about 1kΩ) in series. This resistor needs to have a larger resistance than the stressed line to detect the short circuits at the end of the metal line. The short-circuit monitor lines (sideways and interlayer short circuits) are connected via a 10Ω resistor to monitor the voltage across it when having a short circuit. To do so, during stressing, a small current is periodically passed through the stressed line, and the voltage drop over the 10Ω resistor is periodically recorded versus time by a digital voltmeter. When a significant voltage across the 10Ω resistor is measured, the device is considered to have failed.

The design of reliability test system

The reliability test system is designed around the test chip and the test set-up for 16 devices as described above under test.

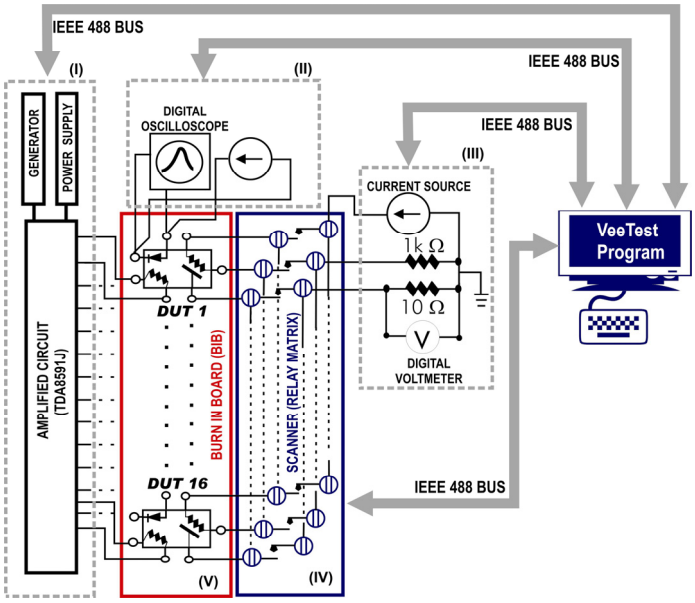


Figure 2.4. *Schematic of the reliability test system for fast thermal cycling test: block (I) is pulsed current source, block (II) is temperature monitor scheme, block (III) is extrusion monitor scheme, (IV) is a scanner like a relay matrix, (V) is a burn in board.*

A scanner (HP 3495A Scanner) is used as a relay matrix that can switch the measurements from one device to other ones periodically, as can be seen on the schematic of the reliability test system showing in Figure 2.4. An amplifying circuit consisting of a TDA8591J (quad BTL audio power amplifier), a power DC source (Delta Elektronika SM 35-45), and a function generator (HP 3314A) is employed to make up the pulsed current source. Thus, the amplitude, the frequency and the duty cycle of the pulsed current are easily variable by changing parameters of the power DC source and the generator. A DC current source (Digistant Type 6750 Calibration Source) and a digital oscilloscope (Tektronix TDS 224) are used in the temperature measurement block. Another DC current source and digital voltmeter (HP 3456A) are used in the device failure detection block. The controlling, the timing, and the data acquisition of the test system are done by a PC connected via IEEE 488 bus and a program written in HP-VeeTest version 6.0. This test system enables a test with 16 devices in parallel. Obviously, the test system can be easily extended for a larger number of devices when the capacity of the equipment is extended.

2.2.3 The use of the test chip

Before performing a FTC test, the most important thing is the calibration of the diode temperature sensor. This section will present how the diode can be used as a temperature sensor. The result of the calibration will be used for reliability tests in section 2.3, demonstrated as an example of the work. Different FTC test conditions that can be achieved by adjusting important parameters such as frequency and duty cycle will be demonstrated.

Diode as temperature sensor

This method is based on Shockley's relation for the current I_F, versus forward voltage V_F, characteristics of an ideal diode. Here, this is only briefly introduced and details can be found in [7]. The forward current of a diode is given by

$$I_F = I_S\left[\exp\left(\frac{qV_F}{kT}\right)-1\right] \tag{2.1}$$

Where, q is the elementary charge, k is the Boltzman's constant, T is the absolute temperature, and I_S is the reverse saturation current. I_S is temperature dependent and can be expressed as

$$I_S = KT^r \exp\left(\frac{-E_{g0}}{kT}\right) \tag{2.2}$$

Where, K, r, and E_{g0} are independent of temperature. E_{g0} is the extrapolated energy gap at absolute zero temperature. In the forward direction $I_F >> I_s$, equation (2.1) can be written as

$$I_F = I_S \exp\left(\frac{qV_F}{kT}\right) \tag{2.3}$$

Most real diodes follow these relations approximately over a limited range of current and experimental results are the best represented by a empirical formula

$$I_F = I_S \exp\left(\frac{qV_F}{nkT}\right) \tag{2.4}$$

assuming, that the diffusion current dominates, we will take the value of n to be 1. Equation (2.3) can be combined with equation (2.2) to get a relation in terms of forward voltage, V_F as

$$V_F = \frac{E_{g0}}{q} + \frac{kT}{q}(\ln I_F - \ln K - r \ln T) \tag{2.5}$$

For temperature sensor application, I_F is kept at a constant, it is easier to write equation (2.5) as the sum of a constant term ($\lambda = E_{g0}/q$), a linear term (γT), and higher-order terms ($O(T^2)$). Equation (2.5) then becomes:

$$V_F = \lambda + \gamma T - O(T^2) \tag{2.6}$$

Where, $\gamma = (k/q)(\ln I_F - \ln K)$, and $O(T^2) = (kr/q)(T \ln T)$. For most practical purposes, the higher-order terms in equation (2.6) can be omitted. Then the relation between temperature T and forward voltage of diode can be expressed as:

$$T = A + BV_F \tag{2.7}$$

the constants A, and B are experimentally determined by using isothermal calibration. The value of B will be called diode thermal coefficient, α_D. It needs to be mentioned that for thermal characterization, the temperature T can be expressed in ^oC. It is observed that the relation (2.7) is generally valid over a small temperature range. For extended temperature ranges, higher order polynomials of the form [8]

$$T = A + BV_F + CV_F^2 + \ldots \tag{2.8}$$

are used. From equations (2.7) and (2.8), the temperature is determined by measurement of diode forward voltage under a constant current during testing.

Calibration procedures of the diode temperature sensor

It is noted that the simplified Shockley's relation is only valid in the exponential portions of the diode characteristic. Therefore, before the calibration, the diode characteristic was measured for different temperatures as shown in Figure 2.5. This is aimed to find a correct current value to operate the diode in the valid region. As can be seen in Figure 2.5 a current in the range of 50μA-150μA is in the exponential portion of the diode characteristic for different temperatures. In this study, a current value of 100μA was chosen to operate the diode for the calibration. It should be noted that this value must be kept the same in the stage of temperature measurement. The calibration is carried out in a chamber of a commercially available DESTIN EM system. The test system has a computer controlled data acquisition, more details can be found elsewhere [9].

The temperatures and diode voltages are sequentially measured over several isothermal steps. The calibration procedure is done as follows; a temperature profile is set with 20°C steps from 60°C to 240°C, and the duration time of each temperature step is 60 minutes.

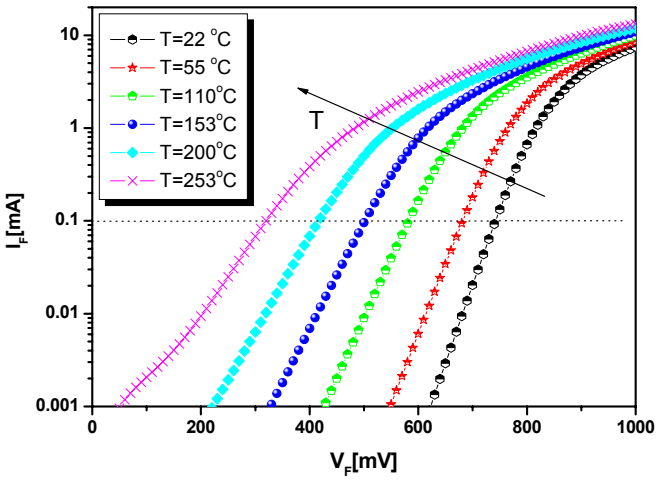


Figure 2.5. *Current versus voltage characteristics of the diode used in this study for different temperatures.*

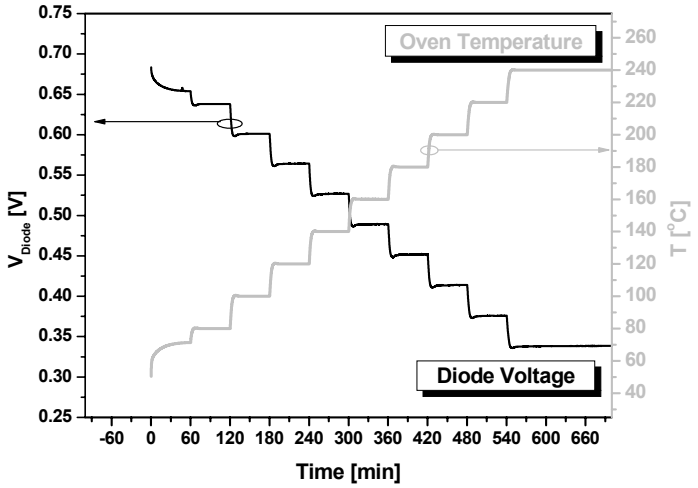


Figure 2.6. *Diode voltage at I_F=0.1mA for different temperatures*

The diode voltages at the current of 0.1mA are sequentially measured with the ambient temperature steps. The measured diagrams of the temperature and the diode voltage over temperature steps are shown in Figure 2.6. The diode voltages at room temperature and at the end of every temperature step are recorded and fitted with equation (2.7) and (2.8). The fitted results are: $T=423.5-0.54V_F$ and $T=408.7-0.48V_F-0.0005V_F^2$. Correlation coefficient of 0.999 was observed for both cases.

Fast temperature cycle condition survey

As mentioned above, the temperature swings can be easily translated from the diode voltage when the thermal coefficient of the diode is known. The temperature swings were measured for different frequencies (10, 20, 40, 60, and 80 Hz) as shown in Figure 2.7a, which were translated from the diode voltage waveform.

Please note that the power amplitude and duty cycle are kept the same at 45W and 10%, respectively for all frequencies. It is observed that the temperature peaks, T_{max} and temperature range, ΔT are lower for higher frequencies while T_{min} increases slowly as demonstrated in Figure 2.7b.

It should be noted that in acceleration test, the higher ΔT's can be achieved with lower frequencies but the number of cycles in a given time is also lower. The duty cycle is also an important parameter to control the temperature profile because it determines the heat-up time in a cycle.

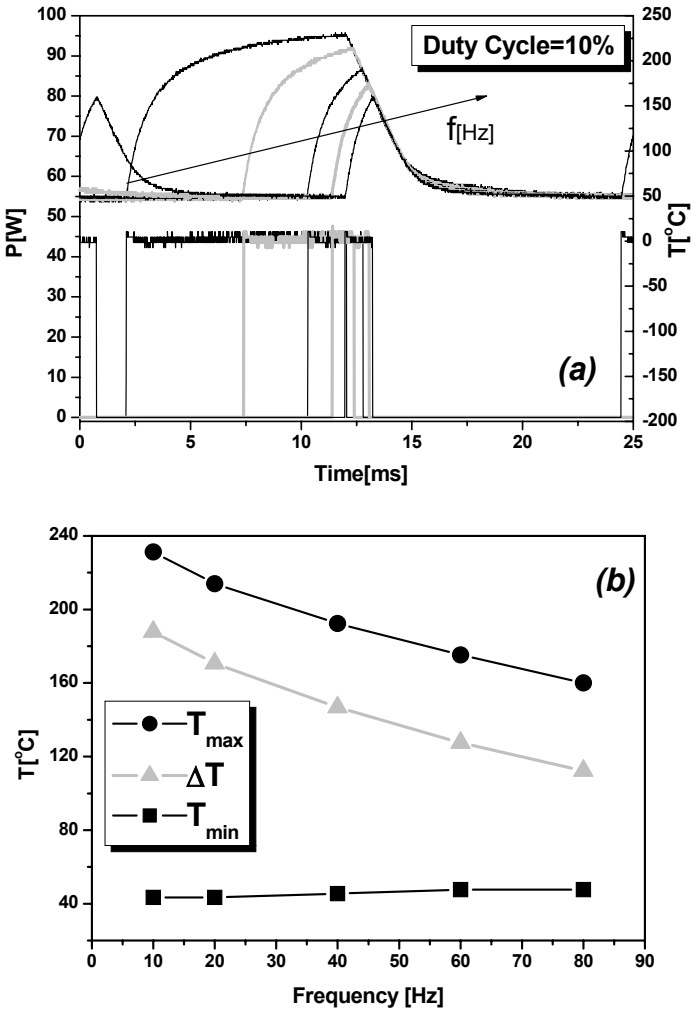


Figure 2.7. *Power amplitude and duty cycle are kept the same for all frequencies, and frequency is varied at 10, 20, 40, 60, and 80Hz:* ***(a)*** *pulsed power and temperature profile;* ***(b)*** *T_{min} , T_{max} and ΔT as a function of frequency.*

The different temperature cycle profiles corresponding to different duty cycles were measured as shown in Figure 2.8a. In which, the power amplitude and frequency are kept the same at 45W and 10Hz, respectively for varying duty cycle, and the duty cycle is varied from 5% to 30% with step of 5%. The plot of T_{min}, T_{max} and ΔT as a function of the duty cycle are shown in Figure 2.8b. It can be seen that T_{min} and T_{max} increase with increasing of the duty cycle, while ΔT does not increase much.

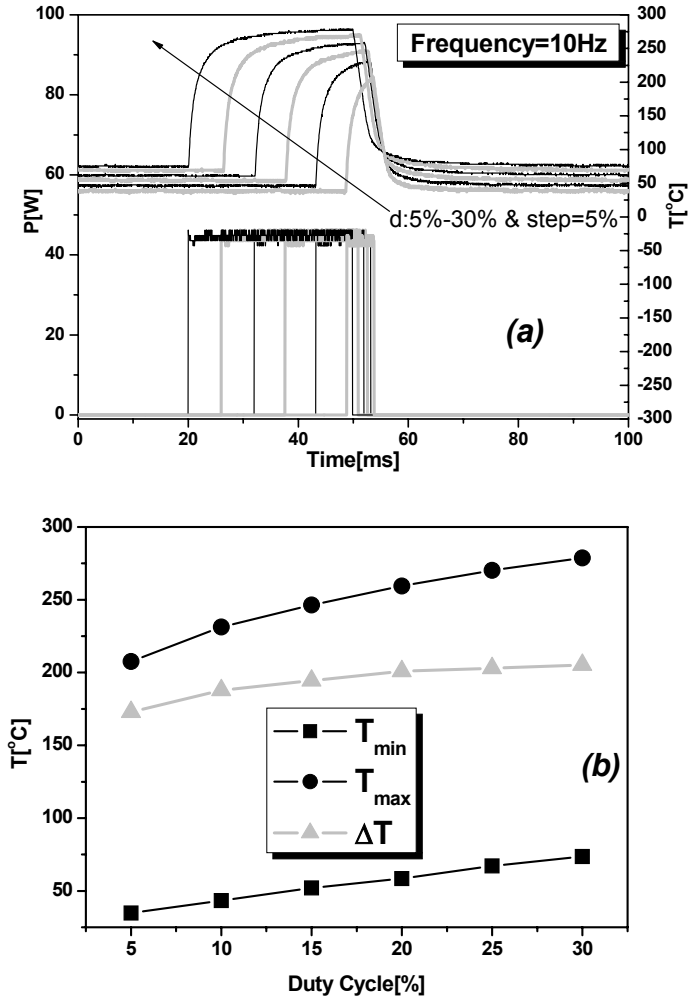


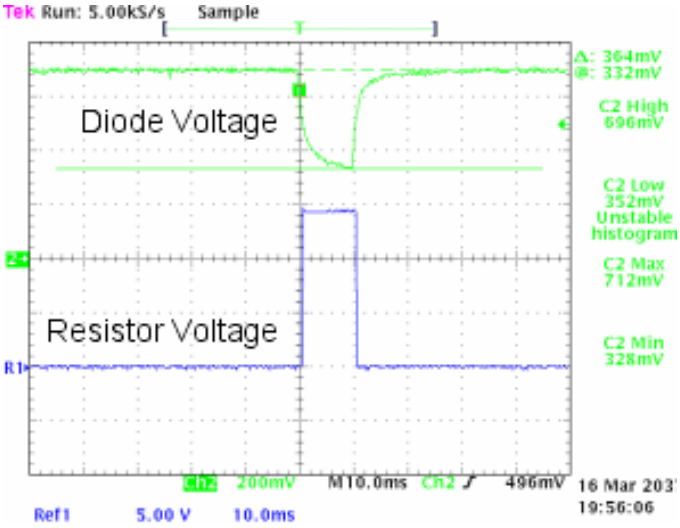
Figure 2.8. *Power amplitude and frequency are kept the same for all duty cycles, the duty cycle is varied from 5% to 30 % with step of 5%:* ***(a)*** *pulsed power and temperature profile;* ***(b)*** T_{min}, T_{max} *and* ΔT *as a function of duty cycle.*

2.3 Reliability tests with fast thermal cycling

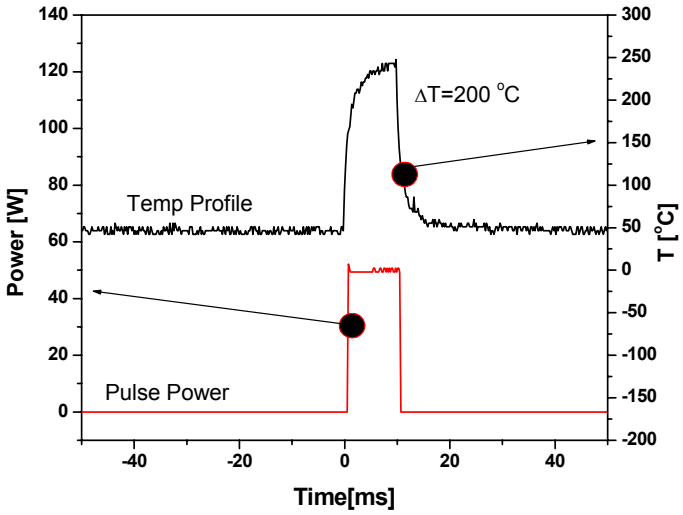
This section presents a study on the reliability of a standard two level metallization of a power IC, using the test chip and the reliability test system as previously described. The reliability tests, the failure analysis, the modelling of failure mechanism, and the development of a reliability mode for the failure rate of the FTC stress will be dealt with, respectively. Finally, a study on the impact of the ILD materials on the reliability of the multilevel interconnects will be discussed.

2.3.1 Experimental details

The reliability tests with FTC have been carried out with three temperature cycle conditions. The minimum temperature was 46°C for all three cycle conditions and the maximum temperature was taken at 266, 246, and 226°C for test conditions A, B, and C, respectively.



(a)



(b)

Figure 2.9. *The temperature profile measured in case of test condition B:* ***(a)*** *the recording of resistor and diode voltages from digital oscilloscope;* ***(b)*** *temperature cycling profile of condition B, only one cycle shown.*

A temperature cycle frequency of 10Hz and a duty cycle of 10% were used for the three conditions. One typical example of the temperature cycle profile that has been measured during the fast temperature cycling test with the condition B is shown in Figure 2.9. The diode voltage waveform correlating with pulsed voltage, captured by a digitalizing oscilloscope, is shown in Figure 2.9a. The temperature profile and pulsed power translated from the recorded data is shown in Figure 2.9b. During thermal cycling, an electrical current of $0.1mA/\mu m^2$ was periodically passed through the stressed line to detect short circuits. This "sense" current should not impose any electromigration-induced damage on the metal line. A sample size of 24 devices was subjected to each condition, and randomized samples from 1 batch were used for these tests. A device was considered to have failed when voltage across the 10Ω resistor due to the short circuit was measured to have a value larger than 1mV. This measurement is taking place every 2 minutes. The time to failure is defined as the time of the first short circuit.

2.3.2 Results and discussions

Figure 2.10 shows a typical result of recorded extrusion monitor voltages. The time to failure can be extracted from that. The failure time data are then analyzed assuming a Weibull distribution, because Weibull distributions are applicable in case where the weakest link, or the first of many flaws, propagates to failure.

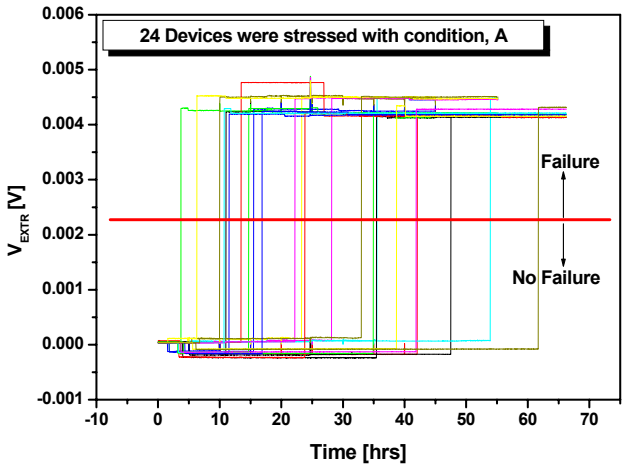


Figure 2.10. *The typical recording of extrusion voltage versus time to show the device failure incase of condition A.*

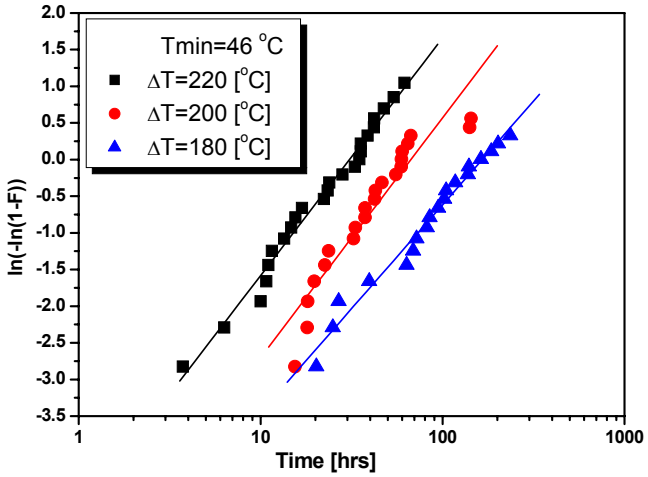


Figure 2.11. *Weibull failure probability plot for fast temperature cycling with temperature ranges of 220, 200, and 180°C.*

Table 2.2. *Results of median time to failure and shape factor*

Conditions	A (ΔT=220°C, T_{min}=46°C)	B (ΔT=200°C, T_{min}=46°C)	C (ΔT=180°C, T_{min}=46°C)
MTF [hrs]	30.8	66.9	165.2
β	1.4	1.4	1.2

Failures due to crack generation, dielectric breakdown, and fracture are typically described by a Weibull distribution [1]. We observed that the failure mode is short-circuiting, which suddenly happens during stressing, indicating a weakest link in the failure mode. By using a least square method of fitting Weibull distribution to time-to-failure data as shown in Figure 2.11, the median time to failure (MTF) and the shape factor (β) were extracted from the three stress conditions. They are summarized on Table 2.2. The distribution parameters are relatively well behaved with similar shape factor, which suggests that failure mechanisms are the same for the three conditions. It is well known that temperature cycling failure mechanisms fit a power law relationship [10], also known as the Coffin-Manson equation as follows:

$$N_f = C_0(\Delta T)^{-q} \tag{2.9}$$

Where N_f is the number of cycles to failure, C_0 is a material-dependent constant, ΔT is the temperature cycling range, and q is the Coffin-Manson exponent determined experimentally. Blish reported that the failure mechanism determines the exponent value [3]. With this in mind, to predict

failure mechanism, the equation (2.9) is used to plot the number of cycle to failure N_f as function of temperature range ΔT for the test results of the three conditions as shown Figure 2.12. The exponent value q is found by using the least square fit to be 8.4. The empirical data in a recent publication data from JEDEC-Standard [11] suggested that the Coffin-Manson exponent values range of 2-4 for metal-related mechanisms and values range of 7-9 for brittle-related mechanisms. Based on the obtained exponent value, it can be deduced that the short circuit failure can be related to cracking of the ILD layer. However, to strongly confirm this failure mechanism, failure analysis was done on several failed devices. To inspect the surface of M1, the plastic package is removed by fuming HNO_3, the passivation layer and M2 are respectively removed by plasma etching and standard chemical etch solution of aluminum, the interlayer dielectric (ILD) is etched using a plasma etcher with end-point detection.

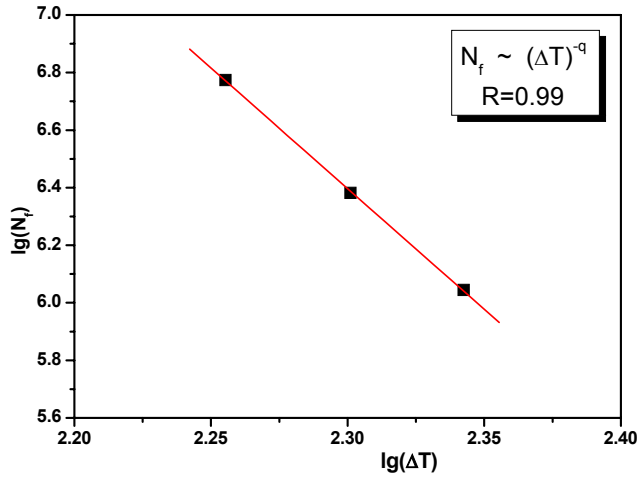
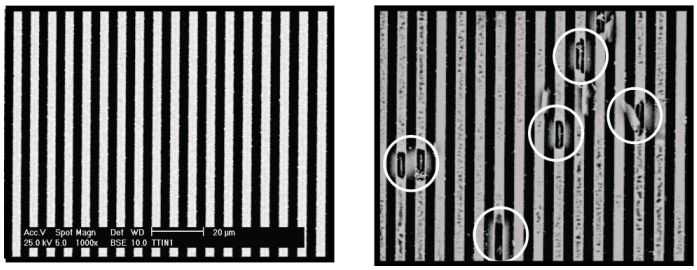


Figure 2.12. *Coffin-Manson plot for three temperature cycle test conditions.*



(a) ***(b)***

Figure 2.13. *The SEM verification of surface of metal level 1, (a) fresh d-vices, (b) more than 100 hours stress with condition C.*

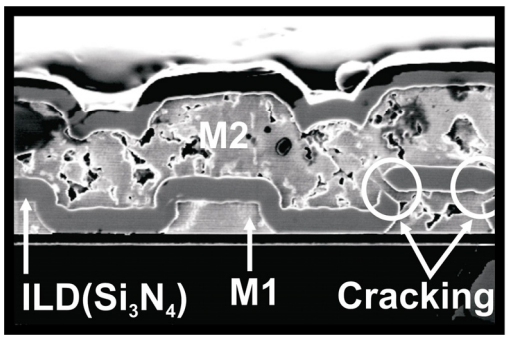


Figure 2.14. *SEM photo of cross-section showing the cracking of the interlayer dielectric due to the temperature cycling stress.*

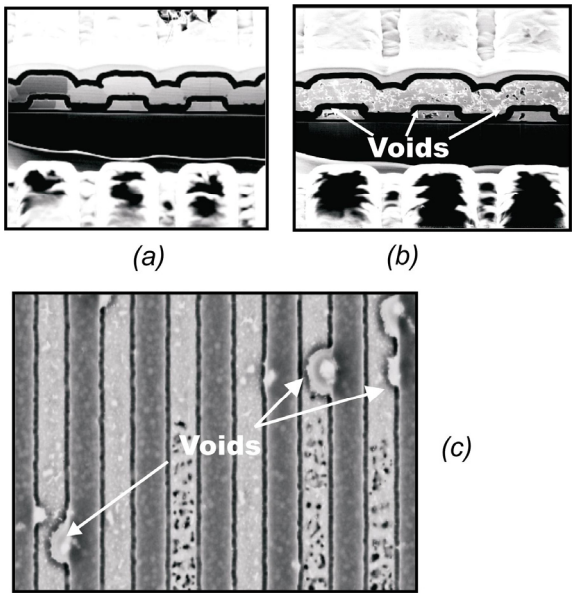


Figure 2.15. *Fast thermal cycling induced voids: (a) Fresh device cross-sections by FBI; (b) Stressed devices cross-section by FIB; (c) SEM image of M1 surface.*

The ILD layer is etched until 200nm is left. Then, the surface of M1 is inspected using a Scanning Electron Microscope (SEM) equipment with a Backscatter Electron (BSE) detector. With this technique, we can avoid damages on the M1 surface due to the sample preparation. The results of SEM verifications on surfaces of fresh and failed devices are respectively shown in Figure 2.13 (a) and (b). Many cracking places on the M1 surface of stressed device but not on the M1 surface of fresh devices were observed. The cross-section of a failed device made by chemical mechanical polishing

and viewed by SEM as shown in Figure 2.14 depicts the cracking of the ILD layer. These observations are consistent with the obtained exponent value as mentioned above. Apparently, another failure mode that can occur is the void-induced open failure during the FTC. Figure 2.15 shows some typical images of voids that have been observed on the cross-section and surface of M1 (see Figure 2.15 (b) and (c)). As can be seen Figure 2.15 (c) the void can grow over the entire line and result in an open circuit. However, this failure mode occurs much later than the open circuit, and it is not possible to detect by an electrical measurement with this test structure. It has been reported in the literature [12][13] that the void-induced by thermal cycling may arise by two mechanisms. First voids may nucleate by a vacancy condensation mechanism. Second, voids may nucleate by the plastic deformation in the metal line.

2.3.3 Failure mechanism modelling

The experiments suggest that the cracking of the brittle materials was the mechanism, and the failure analysis also pointed out that the cracking of the ILD (Si_3N_4) is the reason of the short-circuit failure. In this section, modelling of the failure mechanism is used to understand those observations. Unlike ductile materials, the ILD (Si_3N_4) does not have an intrinsic fatigue mechanism, so why does the ILD cracking occur by thermal cycling loads. Recently, Huang, et al. have investigated the failure mechanism of layer materials on the silicon die under thermal cycling conditions, where cracking in the brittle film is caused by ratcheting in adjacent ductile layers [15]. This mechanism is applied to model the failure mechanism that was observed from the experiment. As can be seen in the Figure 2.16a, the silicon chip is soldered to a lead frame (package substrate) and the surface of the chip is covered with moulding resin (polymer). The packaging substrate has a larger thermal expansion coefficient (TEC) than the silicon chip. Upon cooling down from the bonding temperature, the substrate will contract more than the silicon chip, but the bonding prevents sliding between the substrate and the chip. As a result, shear stresses will develop on the chip surface, concentrated at the chip corner, pointing to the chip center. The chip and the polymer are joined, so that the shear stresses are limited by the yield strength of the polymer. This yield strength is much lower than the yield strength of metal (Al) as well as Si_3N_4.

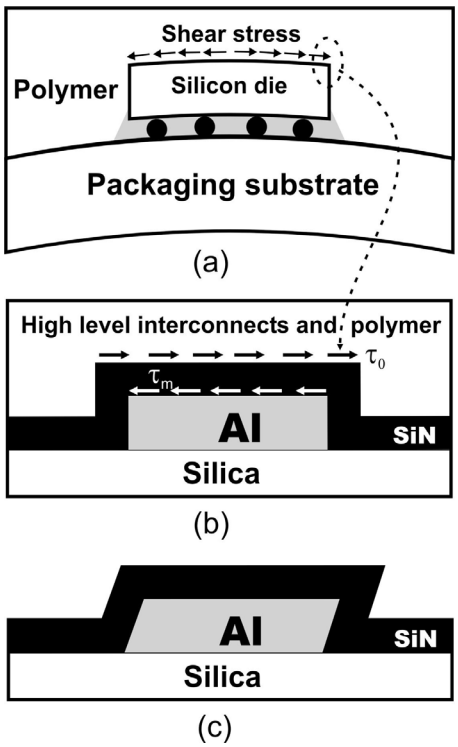


Figure 2.16. *The idealized model for thin film cracking due to fast thermal cycling; (a) contracting of package subject and shear stress builds-up; (b) transferring shear stress from surface to ILD and metal 1 surface; (c) plastic deformation of Al pad.*

This explains why no cracks have been observed before the temperature cycling. It is recognized that the surface shear stress is partly transmitted from the chip surface to the ILD and metal layers with magnitudes of τ_o and τ_m, respectively, as can be seen in Figure 2.16b. These shear stresses are known to depend on different factors such as material properties, temperature conditions and package geometries that were extensively studied by Edwards, et al [16]. For simplicity, the magnitude of τ_o is taken to be constant and the upper level layers are neglected. Before the thermal cycling, the τ_o and τ_m are balanced therefore the Si_3N_4 layer sustains a very small stress, much lower than its fracture resistance. It should be mentioned that the FTC is done at a high range of temperature (high T_{min} and T_{max}) but the T_{max} is present a very short time (ms) and locally so that the direction of τ_o can be approximately considered to be almost unchanged during the FTC. Because of the large difference in TECs among the aluminum, dielectrics and silicon, the metal pad deforms plastically during temperature cycling as reported in an early study [17]. This deformation accumulatively increases in the same direction of

shear stress τ_o due to increasing the number of temperature cycles as can be seen in Figure 2.16c. Consequently, the shear stress in the metal pad τ_m decreases, and the normal stress in the plan of Si_3N_4 layer, which is simply calculated by (2.10) will increase.

$$\sigma_s = \frac{(\tau_o - \tau_m)W}{2t} \tag{2.10}$$

Where, W and t are the width and the thickness of the metal pad, respectively. Equation (2.10) implies that when the shear stress in the metal pad, τ_m relaxes, the Si_3N_4 layer sustains a higher stress build up. When this stress in the films is higher than its fracture strength, K_C, cracking of the ILD layer occurs. The fracture strength of the film is approximated by the following equation [18]:

$$K_C = \sigma_o \sqrt{t/2} \tag{2.11}$$

Where σ_o is residual stress and t is the thickness of the layer. Through the modelling of the failure mechanism, we see that the failure mechanism is strongly influenced by different factors such as temperature conditions, dielectric material properties and the package (moulding resin properties, lead frame, and nature of packaging process).

2.3.4 Reliability model development

The failure mechanism was related to the shear stress from the packaging. This shear stress is generated due to the large difference in the TEC among silicon chip, package subject, and moulding compound used in the assembly. Design, process, and materials all can be used to reduce the shear stress. For instance, in the package process, if the assembly materials have the TEC closely matched to that of silicon, the shear stress would significantly reduce. The magnitude of shear stress, τ_o is strongly dependent on the temperature conditions and temperature of moulding compound of plastic package. This observation has been collected from experimental data in the literature [16,17,19,20].

Originally, the Coffin-Manson equation is used to describe the failure rate for ductile materials as follows:

$$N_f = C[\Delta\varepsilon_p]^{-\alpha} \tag{2.12}$$

Where, $\Delta\varepsilon_p$ is the plastic strain range, which is the difference in strain per cycle, C is a material constant, and α is an empirically determined constant.

The Coffin-Manson equation works well, even for brittle material failure, where failure is dominated by the cracking mechanism [11]. During a temperature cycle, not all of the stress may induce plastic deformation. If a portion of the cycle, ΔT_o, is actually elastic, then this elastic portion should be subtracted from the total strain range.

$$\Delta\varepsilon_p \propto \left(\Delta T - \Delta T_o\right)^b \tag{2.13}$$

Where, ΔT_0 is the portion of the temperature range in the elastic region. Assuming that the failure mechanism is not dependent on the absolute temperature, and the elastic range (ΔT_o) is much smaller than the entire temperature cycle range (ΔT), then combining equation (2.12) and (2.13), the equation (2.10) in the previous section can be obtained. The equation (2.12) works very well for many failure mechanisms induced by the conventional thermal cycle test. Blish's paper [3] summarizes many empirical data from literature on this topic. This equation fits well for the results of the FTC tests with the three conditions A, B, and C as presented in previous section. This is due to the fact that the three conditions A, B, and C have the same T_{min} (this will be explained later). In the literature, Dunn and McPherson reported that the shear stress-induced failure by thermal cycling could not obtain a uniform acceleration factor, in cases the test conditions have the same temperature range but difference in T_{min} and T_{max}[2]. As can be seen from the modelling of the failure mechanism that the failure by FTC stress is also related to the shear stress-induced. This indicates that other reliability tests with the FTC at a higher range of the temperature (higher T_{min} and T_{max}) should be done to verify the fit of Coffin-Manson model for the FTC. After stressing at conditions D and E (see Table 2.3), the results of lifetime distributions are plotted in Figure 2.17. The slope β and MTFs are extracted as shown in the Table 2.3. We observe that the distribution parameters are comparable to those of the conditions A, B, and C. The similar distribution parameter indicates that the failure mechanism is unchanged. However, the MTF's are interestingly different. The MTF is larger by testing under condition D than conditions A, B, and C (see Table 2.2 and 2.3), although the temperature range of condition D is higher that conditions A, B, and C. This makes it impossible to fit with the Coffin-Manson equation, in which MTF is contra-variant function of ΔT. The number of cycles to failure, N_f, is plotted as a function of ΔT for all cases (A, B, C, D, and E) as shown in Figure 2.18.

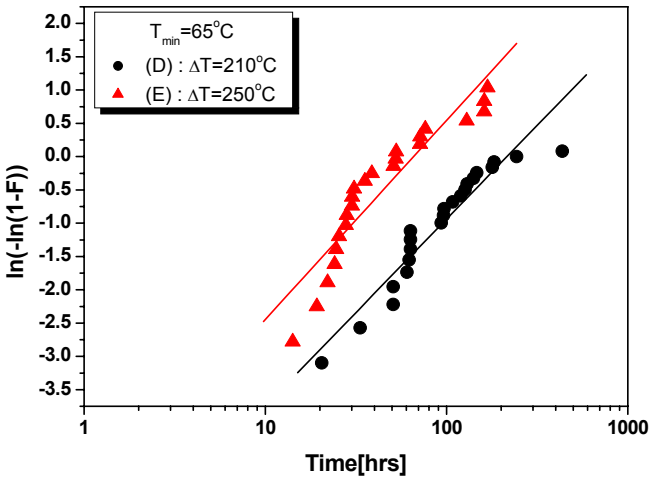


Figure 2.17. *Weibull failure probability plot for fast temperature cycling with ΔT of 250°C and 210°C, and T_{min}=65°C.*

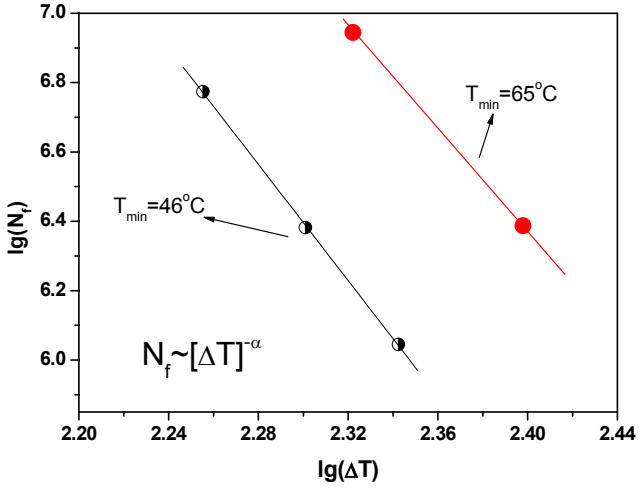


Figure 2.18. *Coffin-Manson plots for different temperature ranges*

Table 2.3. *Results of median time to failure and shape factor*

Conditions	D(ΔT=210°C, T_{min}=65°C)	E(ΔT=250°C, T_{min}=65°C)
MTF [hrs]	193.7	65.8
β	1.0	1.3

It can be seen that not all conditions fall on the same straight line. This means that the Coffin-Manson equation cannot be used to describe the characteristic of the lifetime for all the FTC tests. Therefore, the question arises here why this equation works well for the conventional thermal cycling but not for the

FTC. It can be seen that with the conventional thermal cycling, the soak time of T_{min} and T_{max} are usually equal and T_{min} and T_{max} are normally lower than the bonding temperature (the temperature to solder the silicon chip to the lead frame) [21]. The average temperature (acted as absolute temperature) is therefore calculated as follows:

$$T_{avg} = \frac{T_{\max} + T_{\min}}{2} \tag{2.14}$$

This implies that the T_{min} and T_{max} play an equal role in the failure mechanism induced by the conventional thermal cycling. Consequently, the Coffin-Manson equation that is only based on the amplitude of the temperature range may be good enough to describe the failure rate respect to number of cycle-to-failure as a function of the temperature range.

On the contrary, the FTC is carried out at a higher range, and the T_{max} can be higher than the bonding temperature and the soak time of T_{max} is shorter than that of T_{min}. As a result of this, the T_{avg} cannot be calculated by equation (2.14), and must be calculated by the following equation:

$$T_{avg} = \int_{T_{\min}}^{T_{\max}} f(T)dT \tag{2.15}$$

Where f(T) is the temperature cycle profile. Assume that the temperature cycle is square pulse with duty cycle, the T_{avg} is approximately calculated as follows:

$$T_{avg} = \frac{dT_{\max} + (100 - d)T_{\min}}{100} \tag{2.16}$$

Where, d is duty cycle. It can be seen that in the case of FTC, the T_{avg} not only depends on T_{min} and T_{max} but also on their soak time. Referring to the modelling of the failure mechanism as described above, T_{avg} is a very important parameter that influences the lifetime test results. When the T_{avg} increases, the stresses build up on the silicon chip due to the plastic package will decrease as reported in [19]. This explains why the test results of the FTC at the higher range of the temperature cycle show a longer lifetime.

Usell's model shows that the plastic strain when a chip is cooled down from moulding temperature (T_{mold}) to the operating temperature (T) is function of the T_{mold} as expressed by [20]

$$\varepsilon_c = \int_{T_{mold}}^{T} \frac{\left(\alpha_p(T) - \alpha_c\right)}{1 + \frac{E_c A_c}{E_p A_p}} dT \tag{2.17}$$

Where α_p and α_c are the thermal expansion coefficient of plastic and chip, respectively; E_p and E_c are the effective modulus of the plastic and the chip, respectively; A_p and A_c are the effective cross-sectional area of the plastic and the chip, respectively; and ε_c is the strain in the chip. With the FTC test, the peak temperature is reached in a short time and the heating is done locally. Therefore, the package is under a low temperature and the temperature dependence of α_p and E_p can be ignored. During the FTC, the average temperature can be considered as the operating temperature. Approximately, the strain in the chip can be expressed by

$$\varepsilon_c \propto \left(T_{avg} - T_{mold}\right) \tag{2.18}$$

Since the metal film is bonded to the silicon chip, the strain of the metal film due to the plastic package can be expressed in the same form (the absolute amplitude may be different)

$$\varepsilon_{Al}^{P} \propto \left(T_{avg} - T_{mold}\right) \tag{2.19}$$

During temperature cycling, the metal film (Al) deforms plastically due to the thermal mismatch, Huang et al [22] have shown that the strain can be calculated by:

$$d\varepsilon_{Al}^{T} = \left(\alpha_S - \alpha_{Al}\right) dT \tag{2.20}$$

Where, α_{Al} and α_S are the thermal expansion coefficient of the Al film and the substrate, respectively. During plastic deformation, $d\varepsilon^{T}_{Al}$ is in compression during heating and tension during cooling. Since the Al film is bonded to the substrate, for a given temperature increment, $d\varepsilon^{T}_{Al}$ is always finite [22] so that the film gains a finite strain during the temperature cycling.

With assuming α_{Al} and α_S are not very dependent on the temperature during the temperature cycles from T_{min} to T_{max}, then the strain of Al film can be simply expressed by:

$$\varepsilon_{Al}^{T} \propto \left(T_{\max} - T_{\min}\right) \tag{2.22}$$

This strain is constrained by the compressive stress from the plastic package. Therefore, the total strain must be calculated by subtracting the strain from the plastic package.

$$\Delta\varepsilon_p = \varepsilon_{Al}^{T} - \varepsilon_{Al}^{p} \tag{2.23}$$

A combination of equations (2.12), (2.19), (2.22), and (2.23), gives a new expression for the number of cycle to failure as follows:

$$N_f \propto \left[C1\left(T_{\max} - T_{\min}\right) - C2\left(T_{avg} - T_{mold}\right)\right]^{-q} \tag{2.24}$$

This equation can be used to explain the results, which have been observed from the reliability tests with the FTC. When the FTC test is carried out at a higher range of the temperature, the T_{avg} is higher. Therefore, N_f is higher. This is the explanation for the results of FTC tests under conditions A, B, C and D. To plot N_f as a function of ΔT for all conditions (A, B, C, D, and E), using equation (2.24), the T_{avg} is calculated by integrating the temperature cycle profile of each condition used (2.15) and the moulding temperature of 175°C that was taken from the packaging process. *C1* and *C2* are assumed to have the same value. The plotted result is shown in Figure 2.19. This clearly shows that the new model fits well for all the test results.

The question remains why the test conditions A, B, and C were well fitted with the Coffin-Manson equation as shown above.

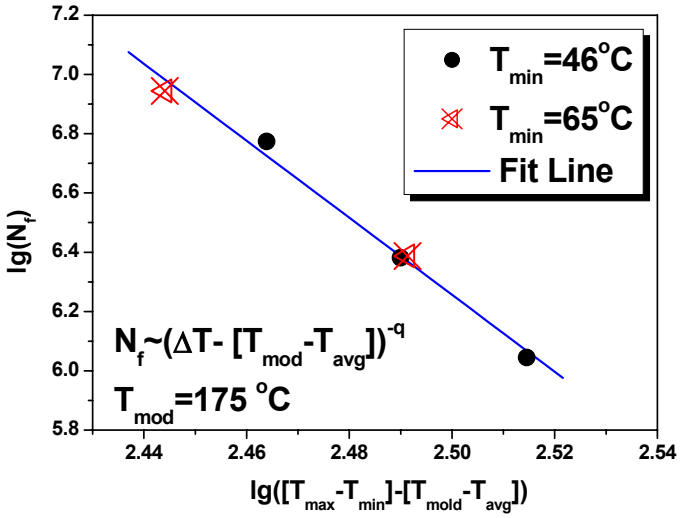


Figure 2.19. *The Log-Log plot of equation (2.24) for all conditions of the fast thermal cycle test.*

Test conditions A, B, and C have the same T_{min}, and duty cycle is 10% so that the T_{avg} is almost the same for the three conditions. This means the equation (2. 22) can be expressed by

$$N_f \propto \left[\left(T_{\max} - T_{\min}\right) + C\right]^{-q} \tag{2.25}$$

Where C is a constant. This equation has the same form as the Coffin-Manson equation. This means that the log-log plot used (2.25) and the Coffin-Manson equation is parallel, maybe with a different offset.

2.3.5 Impact of interlayer dielectric materials

In this section, the impact of the ILD material on the reliability of samples under FTC is studied. The Young's modulus (measure for the elasticity of the material) and fracture toughness are important parameters that can affect the reliability. A layer with a lower Youngs modulus may be deflected locally until it fractures during processing, such as probe and wire bonding, while the lower fracture toughness layer can lead to an early cracking failure due to the building up of larger stress in the ILD layer than its fracture toughness. Collected data from the literature shows that for a range of materials the Youngs modulus and fracture toughness decreases with the decrease of the dielectric constant [18,24]. To verify these observations, the reliability tests with the FTC are done with two ILD materials (SiO_2 and Si_3N_4). These materials have different mechanical properties and dielectric constants (k_{SiO2}~3.9-4.5 and k_{Si3N4}~7).

A new batch of devices were processed, in which for half number of the wafers, PECVD SiO_2 was used as the ILD and for the other half PECVD Si_3N_4 was used. Other than the deposition of the ILD layer all the other processing steps were identical. The thickness's of the ILD layer was chosen at 550nm and 900nm for SiO_2 and Si_3N_4 respectively in order to keep the inter-metal-capacitance constant. The devices were subjected to test conditions A and E (see Table 2.2 and 2.3). The procedure to detect a failure is the same as described in section 2.3. The failure time distributions are plotted in Figure 2.20. It can be seen that the lifetime of sample with Si_3N_4 as the ILD is a larger than that of sample with SiO_2 as the ILD. The lifetime and the slope of the new samples with the ILD of Si_3N_4 (new batch process) are not much different compared to previous devices (see for instance Figure 2.11).

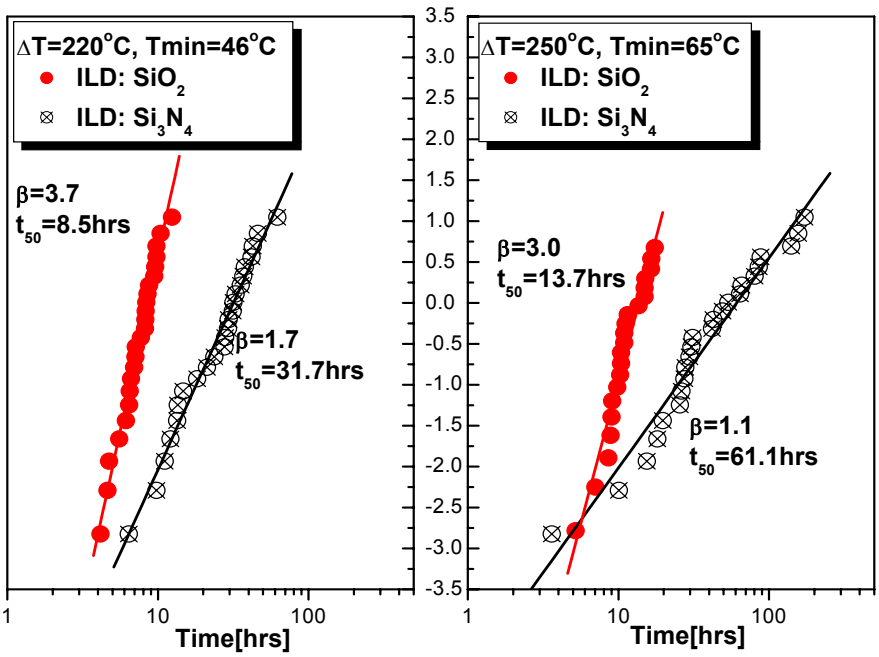


Figure 2.20. *Weibull failure probability plot for fast temperature cycling with test samples with an ILD of Si_3N_4 or SiO_2.*

Table 2. 4. *Typical mechanical properties of SiO_2 and Si_3N_4 [www.goodfellow.com].*

Materials	Young's Modulus [GPa]	Toughness [MPa.m$^{1/2}$]	CTE [10^{-6}/K]	Thermal Cond. [W/mK]
SiO_2	65-75	0.79	0.5-0.75	f(T)
Si_3N_4	150-200	1-4	2.0-3.0	30
Al	70	-	23.5	237

However, the slopes of the samples with SiO_2 are steeper with Si_3N_4 as the ILD for both test conditions A and E (see Table 2.2 and Table 2.3). The reduced thickness of the SiO_2 ILD film could be a main reason resulting in the lifetime reduction of SiO_2 samples. For thinner layers the cracking of the film might occur more sudden resulting in a steeper distribution or the critical stress is reached earlier resulting in a lower lifetime. On the other hand, some mechanical properties of the Si_3N_4 and SiO_2 collected from the literature and as shown on Table 2.4 indicate that the Si_3N_4 would be better to resist the

thermomechanical failure because it has a higher Young's modulus and thermal expansion coefficient (closer to the values for aluminum). It is known that the mechanical properties of the ILD layers are very dependent on the nature of the processing steps. As can be seen in equation (2.9), the fracture toughness of a thin film is a function of the residual stress. Because the adhesion involves the transmission the shear stress to the layers (see the modelling in Figure 2.16). Therefore, a bad adhesion due to the processing steps can also lead to a shorter lifetime for the SiO_2 samples. Another possible explanation for the shorter lifetime of the SiO_2 samples is that the process with Si_3N_4 as the ILD is currently used in the standard process flow for power ICs at a fab. Therefore many optimized process steps were done. The SiO_2 on the other hand is just introduced as the ILD for this study. To further understand the effect of ILD thickness or mechanical properties of ILD materials on the fast thermal cycling lifetime, more experiments are needed, which are beyond of this thesis. However, the important feature of this experiment is that a change in ILD material might result in a change in lifetime. This might also affect the reliability of Cu/low-k advanced metallization schemes. Low-k dielectrics have poor thermal and mechanical properties. Thermomechanical failures arising from the thermal cycling are a concern because thermal cycling experienced during thermal excursion encountered in processing steps or during usage are unavoidable. As further IC downscaling of Al or Cu interconnects urgently requires the implementation of the low-k materials, temperature cycling related reliability studies are therefore much needed.

2.4 Conclusions

The fast thermal cycle test method has been studied and a typical application for fast reliability testing of interconnects for power ICs has been presented. The test chip and the reliability test system for the fast thermal cycling test have been represented. This test method shows that it can enable quick assessments of reliability in qualification test for microelectronics, regarding thermomechanical failure.

Reliability tests on a standard two level metallization with the fast thermal cycling under different conditions have been studied. It is found that the lifetime is not only dependent on the temperature range (ΔT), but also dependent on the average temperature. The Coffin-Manson equation can be

only used for the test conditions, which have the same minimum temperatures. The exponent value indicated cracking of the interlayer dielectrics, which was confirmed by failure analysis. The driving force for the failure has found to be related to the packaging shear stress and plastic deformation during the thermal cycling, which has been shown through the modelling of the failure mechanism.

A reliability model has been successfully developed that can be used for all test conditions of fast thermal cycling. Therefore, it can be used in predicting reliability under the use condition. This model shows that the lifetime is strongly dependent on the nature of package process and the range of the test temperature.

The effect of the ILD materials on the reliability of the multilevel interconnects has been addressed with two conventional dielectrics PECVD SiO_2 and Si_3N_4 to obtain an indication of thermomechanical issues with going to advanced low-k dielectric materials.

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CHAPTER 3

Fast Thermal Cycling Enhanced Electromigration

CONTENTS

As presented in chapter 2, fast thermal cycling can cause cracking of interlayer dielectrics, resulting ultimately in the destruction of multilevel interconnects, if not it can degrade the thin films such as passivation, interlayer dielectric, and metal layers. In the field use condition, the devices are operated under a combination of fast thermal cycling and electrical current stresses. Therefore, these degradations could promote in early failures due to electromigration, especially due to electromigration-induced extrusion-short failure mechanism. This chapter will present a study of electromigration-induced extrusion short circuit failures and its enhancement by fast thermal cycling stresses. Electromigration tests have been performed under different conditions. The extrusion failure mechanism is investigated and explained in detail. Application of a no-cracking condition, electromigration simulation, and thermal stress simulation of the device are used to fully understand the failure mechanism. Electromigration tests on devices encapsulated in different plastic packages show a difference in the lifetime. To study the influence of fast thermal cycling on the electromigration lifetime, subsequent electromigration tests on devices pre-stressed with fast thermal cycling have been carried out. With the introduction of fast thermal cycling as preconditioning, the electromigration lifetime is significantly reduced. This reduction is found to be dependent on the minimum temperature and the temperature range of fast thermal cycling.

3.1 Introduction

Electromigration (EM) is a phenomenon that occurs when electrical current leads to mass transport of metal atoms within integrated circuit (IC) metallization [1]. EM-induced failure of interconnects can be either voids growing over the entire line width that cause breaking or resistance increase of metal line or extrusions that cause short circuits to neighbouring metal lines. Many extensive studies have been reported about EM-induced open circuits as well as the resistance increase failure mode in submicron line metallization. However, the EM-induced extrusion short circuit as demonstrated in Figure 3.1, which has been already reported in an earlier study [2], can become a reliability concern in modern integrated circuits, where multilevel metallization schemes with faster, smaller and higher performance are required. This means that the multilevel interconnection dimensions, linewidth, linespacing, and junction depth are shrunk to accommodate a higher density of metal lines, and low-k dielectric materials are introduced to increase the speed. As reported in literature, low-k dielectrics have worse mechanical properties compared to conventional dielectrics [3]. Metallization schemes using low-k materials as an interlayer dielectric (ILD) can cause a reliability problem because of metal extrusion due to a compressive stress induced by an EM driving force [4]. In these cases, the use of design rules based solely on open circuit failure mode could result in a less reliable product. It has been recognized that the extrusion short circuit induced by EM that results in the cracking of ILD (or passivation) not only depends on the metallization properties but also on the ILD properties.

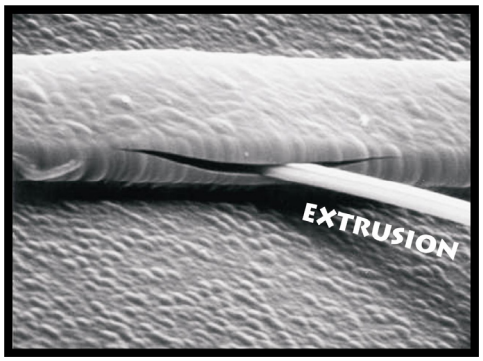


Figure 3.1. *SEM image showing a extrusion of metal through passivation*

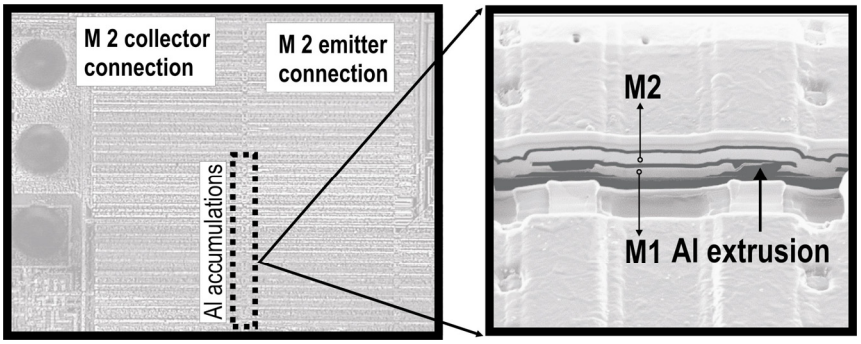


Figure 3.2. *A typical example of power IC failure due to Al accumulation by electromigration: (a) showing the accumulation of Al at the collector tracks; (b) FIB cross-section showing the extrusion short circuit between metal1 and metal2.*

For instance, if a lower elastic modulus ILD is used, it could flex and relieve some of the compressive stress induced by EM in the metal line, and the EM extrusion could be delayed accordingly. It can be seen that the thermal and mechanical stresses can degrade the metal line (induce voids) as well as the ILD (induce micro-cracks). With this connection, the effects of the thermal and mechanical stresses generated in both the ILD and the metal layers due to the thermal mismatch between metallic, dielectric and silicon substrate is a particularly important aspect to the EM-induced extrusion failure mechanism.

It is known that in power IC metallization schemes, there is a coupling between thermal and electromigration stresses due to large AC signals. Therefore, a combined stress of EM and thermal cycling may induce early extrusion failures in the metallization, which would be a major reliability concern in power IC's. A typical example of extruded metal failure in commercial power ICs is shown in Figure 3.2. The accumulation of Al in collector tracks due to EM resulted in a short circuit between metal 1 and metal 2. Apparently, this failure could be due to a combination of electromigration and thermal cycling stresses. There are quite some studies about the effect of thermal cycling on the EM performance [5,6]. In these studies, the thermal cycling is done slowly using an environmental chamber. The typical temperature cycle time for this method is quarters of an hour or more. This possibly masks the mechanism of more realistic fast thermal cycling (FTC) on the EM performance. Furthermore, the effects of the FTC on the EM performance is still unknown so far, and a full understanding the effect of the FTC stress on the EM performance are necessary to adjust the EM design rules for a better reliability of multilevel interconnect in power IC's.

In this chapter, characterization of the EM-induced extrusion short-circuits mode of a standard two level metallization currently used in power IC's will be presented in detail. A no-cracking condition together with simulations of compressive stress induced by the EM and the thermal expansion is used to demonstrate the failure mechanism. The impact of two different plastic packages on the EM-induced extrusion failure is examined. In particular, the influence of the FTC induced by the on chip micro-chuck on the EM performance is investigated, in which different FTC conditions are employed to carry out the preconditioning to distinguish between the effects of FTC temperature range (ΔT) and FTC minimum temperature (T_{min}) on the EM lifetime for two package types.

3.2 Experimental details

In this study, the same design of test chips as described in chapter 2 is used. The metal line (metal 1) has Kelvin contacts to accurately measure the resistance, which is used for conventional EM testing. The EM test structure is similar to the one proposed by the National Institute of STandards (NIST) for EM testing.

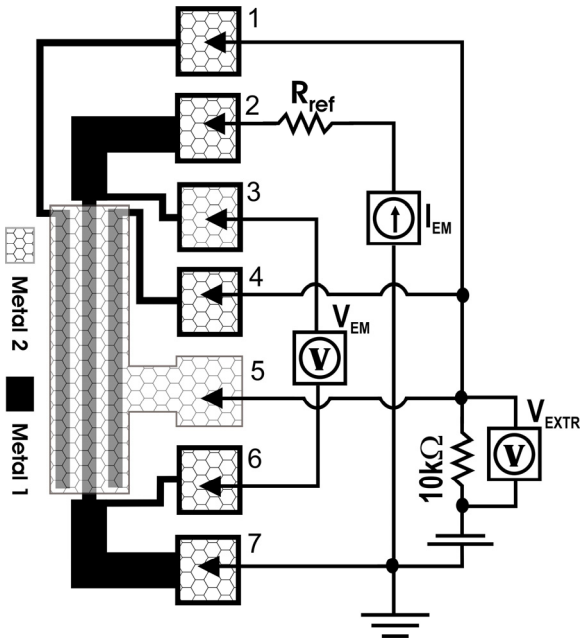


Figure 3.3. *Top view diagram of the electromigration test structure together with the electromigration test circuit; pads (2), (3), (6) and (7) are I^{+}_{EM}, V^{+}_{EM}, V^{-}_{EM}, and I^{-}_{EM}, respectively, and (1), (4) and (5) are extrusion monitors.*

However, the stressed line has additional tracks at both sides to monitor lateral extrusion in metal 1 and a large metal 2 plate, covering the entire structure, to monitor interlayer metal extrusions during the EM testing. The geometry of the EM test structure can be seen in Figure 3.3. The test chips were processed with a standard two level metallization using Al alloy (Al-Si 1%-Cu 0.5%) and encapsulated in standard 17 pins power packages (DBS-17-P). Two different packages referred as type A and B were used. The essential differences between type A and B are as follows; with the package type A, a polymer die-attachment has been used to glue the silicon die to the lead frame, and with package type B, lower stress moulding compound and solder die-attachment have been used.

To perform EM tests, a commercial set-up (DESTIN EM system with temperature stability of 0.02°C and current stability of 250ppm) has been employed. The basic EM test circuit schematic used in this work can be seen in Figure 3.3 where the test circuit is mounted with the EM test structure. A constant current is passed through the metal line and the voltage across the metal line is monitored. The three extrusion monitors are supplied via 10kΩ. During EM testing, the resistance of the stressed line and the extrusion voltage across on the 10kΩ resistor are continuously monitored. By connecting the 10kΩ resistor and the extrusion monitors in series, the current through the stressed line remains the same even after the first extrusion is formed. To carry out a pre-stress with the FTC, the experimental technique for the FTC test that has been described in chapter 2 is employed.

3.3 Results and discussions

This section is split into two subsections, first the EM-induced extrusion failure mode is discussed and secondly the effect of FTC on the EM performance is studied.

3.3.1 Electromigration-induced extrusion failure mode

Conventional EM tests were carried out to examine the EM performance of metal 1. Fresh devices encapsulated with the package type A were tested with condition E1, E2, E3, E4, and E5 as shown in Table 3.1. For each stress condition, a sample size of 16 devices was used. The samples were stressed more than 1500 hours. Figure 3.4a and Figure 3.4b show typical resistances of the stressed line measured as a function of time in case of EM tests with the

conditions E2 and E4, respectively. It can be seen that there is the absence of gradual increase in the resistances. A slight reduction of the resistances at the beginning is due to a further alloying of metallization. The resistances drop due to an extrusion (explained in the text) is observed for condition E2 but not for condition E4. Actually, the absence of gradual increase in the resistances was observed during all other stress conditions, so gradual resistance increase cannot be a failure criterion for these samples.

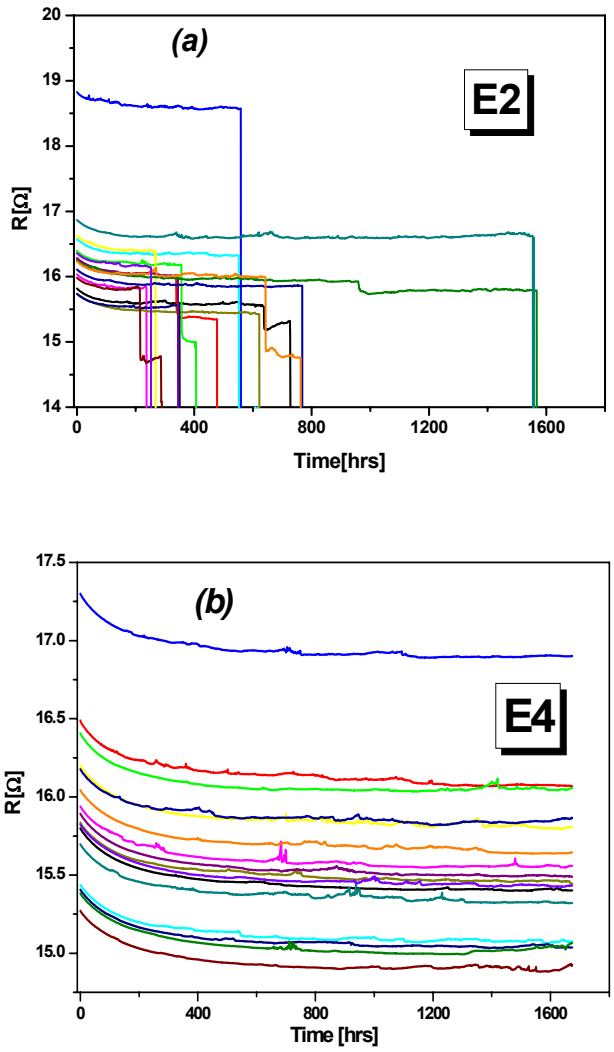


Figure 3.4. *Resistance evolution of metal lines stressed with condition:* ***(a)*** *E2, extrusion failures are observed;* ***(b)*** *E4, no failure is observed.*

Table 3.1. *Electromigration test conditions*

Name	J [mA/μm^2]	T [^{o}C]
E1	25	125
E2	25	150
E3	15	125
E4	15	150
E5	25	175

In addition, alloying of the aluminum with solutes of Cu, using many optimized steps in deposition processes was introduced to increase the EM resistance of the metal line. When considering extrusion fails, the situation changes. Except for the low stress conditions E3 and E4, we observe that devices fail due to extrusions, and only few devices are open circuit at the end (as will be explained later). Typically, the extrusions happen before the open circuit as shown in Figure 3.5a. The open circuit did not always occur because the current in the stressed line can be reduced too much due to the extrusions. In Figure 3.5b, a zoom-in shows more visible the simultaneous variations between resistance of the stressed line and voltage of an extrusion monitor. It can be seen that the first extrusion has been formed, and the resistance of the stressed line did not change. This means that the stressed current remains in the stressed line at this moment, and the test is continued until another extrusion or open circuit. When the second extrusion forms, which can be observed from the measurement of extrusion voltage (see Figure 3.5b), the resistance of the stressed line shows a drop because a portion of the stressed line is shorted out by the two extrusions. It can be also seen in Figure 3.5b that before the second extrusion there is a slight increase of the resistance of the stressed line as well as the extrusion voltage due to the larger extrusions. With a long time stress, the resistance of the stressed line could drop steeply (see Figure 3.5b). As demonstrated in Figure 3.3, the extrusion monitor pads were connected together during the EM testing for the extrusion monitor. Therefore, to distinguish between sideways extrusion (the extrusion of stressed line to sideways tracks) and interlayer extrusion (the extrusion of stressed line to metal 2), separated sequential extrusion monitors of the sideways extrusions and the interlayer extrusions were carried out on the failed devices. We found that only the interlayer extrusion was observed in most cases. This implies that the interlayer extrusion (the extrusion between metal 1 and metal 2) is the main failure mechanism in these samples.

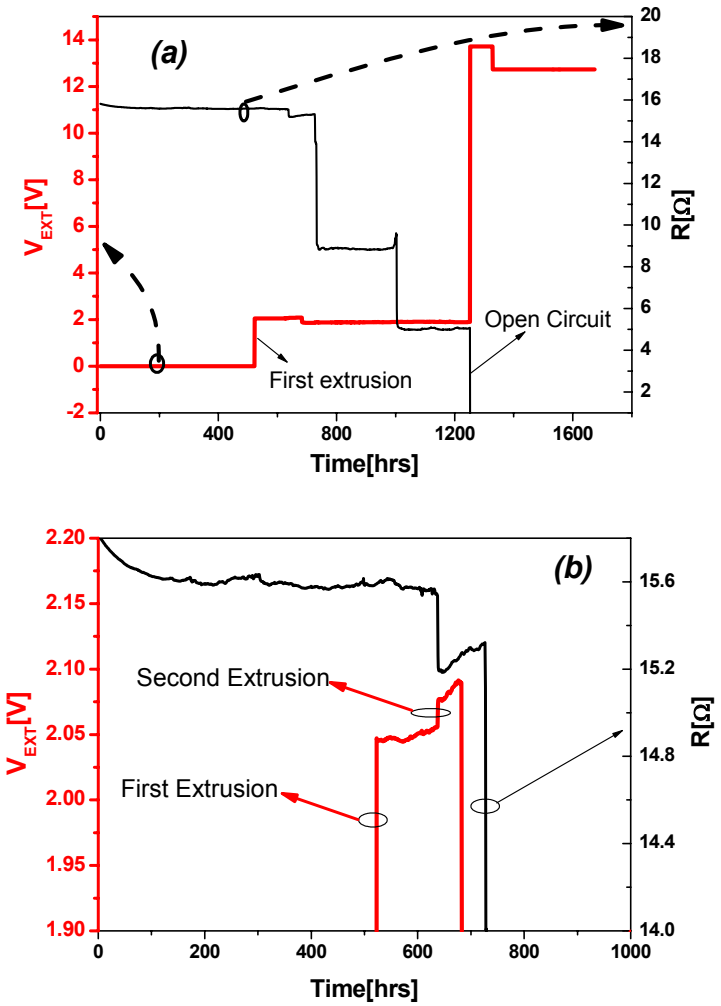
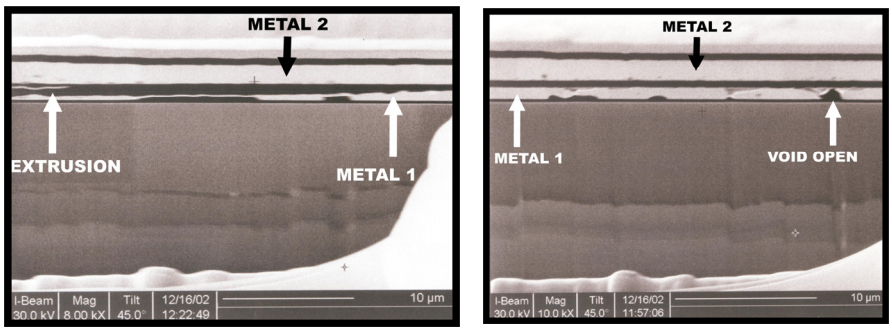


Figure 3.5. *Monitor results of metal line resistance and extrusion voltage:* ***(a)*** *A typical extrusion and resistance measurement of a sample for the whole electromigration period:* ***(b)*** *A zoom-in of the first extrusion to show in details the extrusion and resistance measurement.*

In order to confirm these observations, the devices with extrusion short circuit and void-open circuit failure identified by the electrical measurement were selected for failure analysis. The structure used in this work has a very thick metal 2 covering over the stressed line and the extrusions are normally very small. Therefore, locating the extrusion is a very difficult task. Several techniques to locate the extrusion such as liquid crystal hot spot detection and optical beam induced resistance change (OBIRCH) have been tried but without success so far, the later technique seems to be promising but more

studies are needed. To overcome this problem, Focused-Ion-Beam (FIB) was used to make cross-sections for searching extrusions and opens on the stressed line. To do so, very long cross-sections were made parallel with the stressed line, which is a time consuming and costly task indeed. After making several cross-sections, we finally observed a typical extrusion and void as respectively shown in Figure 3.6a and 3.6b. Please note that the extrusion as shown in Figure 3.6a did not show clearly the extrusion short circuit between metal 1 and metal 2, which is very difficult to obtain by making cross-sections because the extrusions are very small. However, Figure 3.6a shows the metal only extruded through the ILD half way to metal 2, but it clearly shows how the extrusion has been formed.

To analyse the EM lifetime in this work, instead of using a given percentages of relative resistance change as is commonly used for electromigration testing, the extrusions short-circuit as mentioned above is used as the failure criterion to estimate the time to failure. This means that a device was considered to have failed when a significant extrusion voltage (larger than 0.1V) had appeared on the extrusion monitor, it should be mentioned that the time to failure is determined by the time to form the first extrusion. In fact, a competition takes place between many locations (micro-crack or defect of ILD) where metal can extrude and cause the short circuit fail. This resembles a weakest link mode. Therefore, the times to failure distributions of the EM tests with conditions, E1, E2, and E5 (see Table 1) were plotted in a Weibull graph, shown in Figure 3.7. It can be seen that the distributions are relatively well behaved with generally similar slope.



(a) ***(b)***

Figure 3.6. *FIB cross-section showing the extrusion-short* ***(a)*** *and void-open circuit* ***(b).***

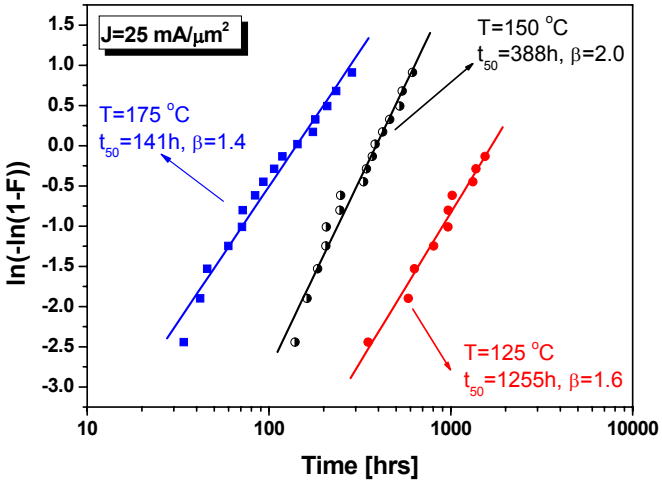


Figure 3.7. *Failure probability plots for electromigration with a current stress of 25mA/μm² and temperatures of 175°C, 150°C and 125°C was package type A.*

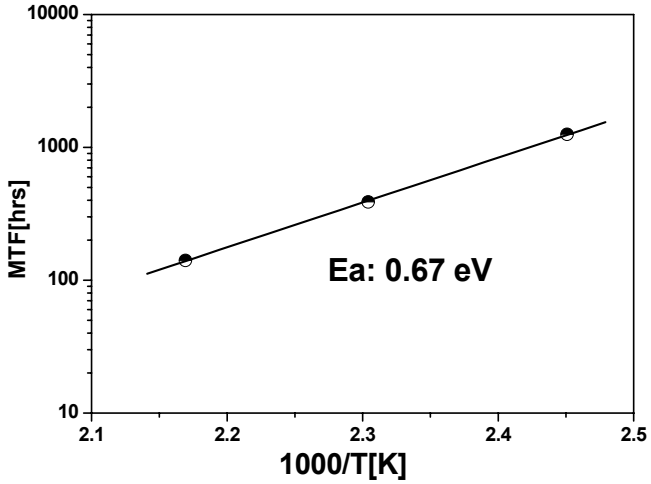


Figure 3.8. *Arrhenius plot of short circuit failures for three temperatures at a current density of 25mA/μm².*

This would imply that the same failure mechanism has occurred for the three test conditions. Figure 3.8 shows the resulting MTF as a function of reciprocal temperature. The temperature rise due to the Joule heating of about 10°C was added to the stage temperature to more accurately represent the stressed line temperature during testing. The activation energy for this failure mode is extracted to be 0.67eV. This value is not much different from the value of around 0.7eV, which has been obtained from original EM process qualification using the resistance increase as failure criteria. These

values of the activation energies are typical of electromigration-induced failure and are consistent with Al-alloy grain boundary diffusion. The similarity in activation energy for resistance increase and extrusion-short failure modes implies that the fundamental mechanism does not change in EM-induced extrusion short circuit. The EM-induced extrusion failures as well as the EM-induced resistance increase are driven by the transport of mass induced by the stressing current. However, the actual failure is caused by the accumulation and depletion of mass at certain places that is affected by the microstructure of the metal line. The movement of Al atoms in the direction of the electron current causes mechanical stresses to build up in the metal line due to atomic flux divergence at grain boundaries, at the anode and the cathode. Tensile and compressive stresses are generated in regions of mass depletion and accumulation respectively. When the compressive forces generated in the metal lines cannot be relieved, they will build up to a point where the dielectric cracks and metal extrudes through the opening. It can be argued that the EM-induced extrusion failure can be assisted by local increase in temperature and the presence of initial voids. Because local heating can cause a micro-crack in the ILD due to the different thermal expansion of the layers where the metal easily pumps through the ILD by the EM stress, and an initial void can cause the current density to increase in the vicinity around itself because of the reduction of cross section area of the conductor.

Recently, Suo [9] has proposed a no-cracking condition for small objects, using fracture mechanics as an energy criterion that can be used for the EM case as follows:

$$\beta P_{\max} \sqrt{W} < K_c \tag{3.1}$$

Where, P_{max} is maximum hydrostatic pressure in the metal line, β is a dimensionless geometric parameter, W is a characteristic dimension of the interconnect cross-section, chosen to be the line-width. K_c is the fracture resistance of the layer overlaying the metal line. Suo has predicted that if the stress build-up at the anode reaches about 1.5GPa, the no-cracking condition will no longer be satisfied resulting in the cracking of the SiO_2 passivation. Chiras and Clarke have presented an extensive study of applying the Suo model for the metal line with Si_3N_4 passivation [10]. They reported that the stress induced by electromigration is only about 1GPa. The thermal stress

due to the thermal expansion mismatch between aluminium and Si_3N_4 at the EM test temperature must be included into the no-cracking condition. The difference in prediction of maximum compressive stress (Suo: 1.5GPa and Chiras: 1GPa) to induce the cracking of the passivation is caused by the fact that they used different passivation materials (SiO_2 and Si_3N_4), and the fracture toughness of SiO_2 which is almost twice as that of Si_3N_4 [11]. Suo and Chiras measured the stress at the anode and taken that as the maximum stress in the line to verify the no-cracking condition.

However, we have carried out failure analysis on many failed devices and did not find any extrusions or cracking of the ILD at the area near anode but the extrusions were found in the stressed line quite far a way from the anode. The explanation is that the vias are filled with Al so that metal diffusion is not stopped at the vias. This implies that the extrusions that were observed are not due to accumulation of material just at the anode. Depending on the microstructure of the metal line, the maximum compressive stress builds up at either anode or a grain boundary (it can be near-bamboo grain boundary with a tripe point or bamboo grain boundary). This means that there is a competition between the failure sites.

To verify this issue, a 2D EM simulator has been used to study the mechanical stress evolution in time of the stressed line with stressed condition E2 ($J=25mA/\mu m^2$ and $T=150^oC$) for different microstructures in the metal line. Details about this simulator can be found elsewhere [12]. The simulation structures were designed with different microstructures, which are bamboo and near-bamboo (triple point) grain boundaries in the metal line as shown in Figure 3.9. Note in these simulations, the activation energies for vacancy diffusion in bulk (E^a_{bulk}) and for grain boundaries (E^a_{gb}) were roughly taken so that they are respectively higher and lower than experimentally obtained activation energy ($E^a_{exp}=0.7eV$) because the activation energy estimated from the experiment depends on the grain boundary as well as bulk diffusion. Furthermore, the aim of these simulations is not quantitative comparisons, but for failure mechanism explanation. Therefore, E^a_{bulk} and E^a_{gb} were respectively taken to be 1.4eV and 0.6eV, respectively. Other relevant parameters for the simulator can be found in [12]. Results of mechanical stress distributions of the metal lines stressed with condition, E2 for 500 hours are shown in Figure 3.10a and Figure 3.10b that are respectively with bamboo and near-bamboo microstructures in the metal line.

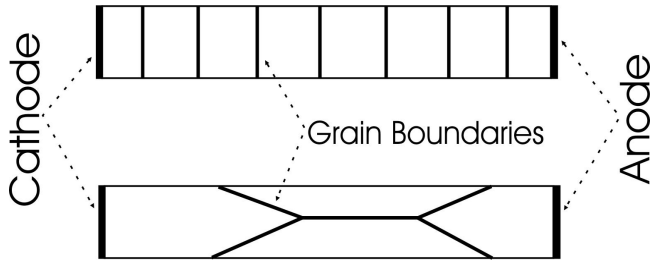


Figure 3.9. *The simulation structures with different microstructures (bamboo and near bamboo).*

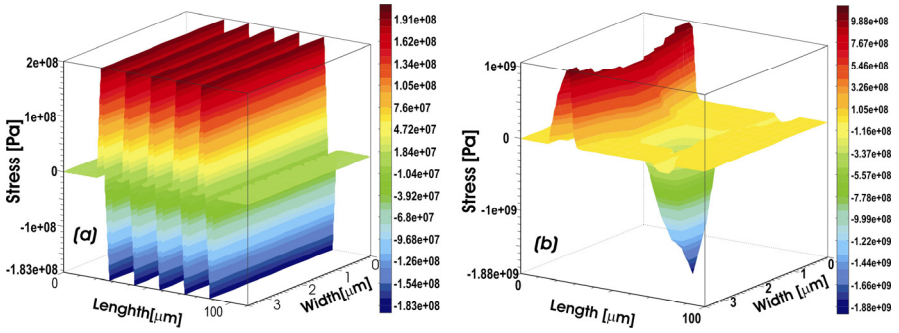


Figure 3.10. *Simulation of stress build-up in metal lines after 500 hours of EM stress (J=25 mA/μm² and T=150°C);* ***(a)*** *is a bamboo grain boundary,* ***(b)*** *is a near bamboo grain boundary.*

Note that the stress builds up very fast at the triple point. Hence, these triple points are the weakest point i.e. the point where the cracking of the ILD and the subsequent extruding of metal can cause a short circuit between metal 1 and metal 2. The maximum of compressive stress at the triple point is 1GPa. As mentioned above, the thermal stress at the EM test temperature, which is a compressive stress in the metal line (because Al has a larger thermal expansion coefficient than both the dielectric and the substrate) needs to be added to the no cracking condition. As seen in published data [13][14], the thermal stress depends on the aspect ratio of the line, the geometry of the interconnect structure, the mechanical properties of the dielectric and the temperature, and its magnitude can be more than 100MPa. To estimate the thermal stress of our sample at the temperature of EM test, a semiconductor process simulator (SILVACO) has been used to simulate the processing of test structure and thermal stress at different temperatures [15].

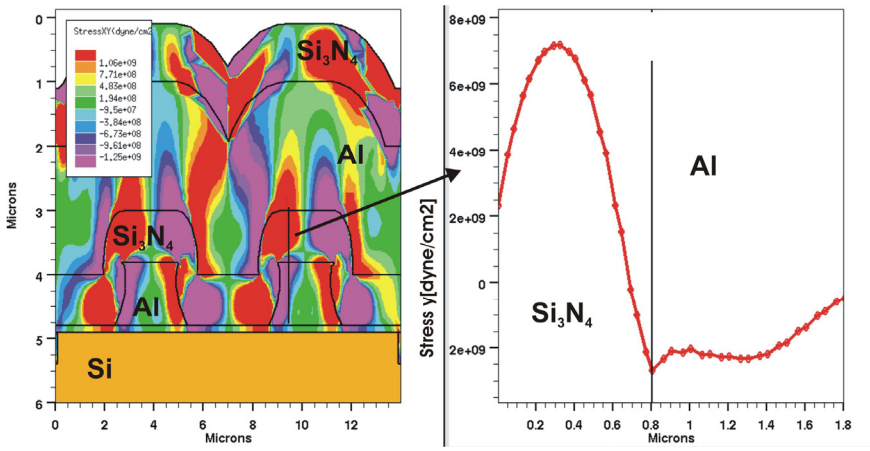


Figure 3.11. *Thermal stress due to thermal expansion mismatch due to an increase from room temperature to the EM test temperature of 150°C.*

First, the processing of the test structure was done following experimental process steps, and the result of simulation as shown in Figure 2.2 of chapter 2. Then, this simulation structure is used to simulate thermal stresses due to the thermal mismatch among the layers due to increasing the temperature from room temperature (23°C) to EM test temperature (150°C). It should be mentioned that the thermal stress of the package (due to the thermal mismatch between package substrate and silicon die) was not included in this simulation. Figure 3.11a shows the thermal stress distribution in layers and Figure 3.11b shows the thermal stress build up in the ILD (Si_3N_4) and metal 1(M1) at the position near the left edge of the metal line. Note that the maximum compressive stress in the metal line is about 225MPa, and this stress can be larger when the thermal stress of package is included. Therefore, the thermal stress cannot be neglected in the no-cracking condition. To verify the no cracking condition for our case, the representative values β=0.3, K_c=0.5MPam$^{1/2}$ and W=3.5μm are taken [10]. Substituting these values to the equation (3.1), we have found out that if P_{max} is lower than 0.9GPa, there will be no cracking of the passivation layer. However, it can be seen that this value is much lower than the total stress (induced by the EM after 500 hours and the thermal stress at the EM test temperature) about 1.2GPa. It should be noted that this thermal stress could enhance the stress gradient due to the EM and would lead to higher back flow vacancy diffusion, consequently reducing the EM. However, the line length is much larger than the Blech length so this effect can be minimal.

In case the metal line is assumed to fail due to the increase of the resistance only, the metallization would be reliable enough for integrated circuit devices. However, cracking of the ILD followed by extruding metal during EM stress could be a persistent failure mode. This failure mode can be affected by different factors, such as the initial void density in the metal line, thermal stress, packaged stresses, plastic deformations characteristics of Al (determined by microstructure and impurity concentration in Al films), properties of the ILD materials (fracture resistance), etc. Another, very important aspect in power ICs, namely fast thermal cycling stressing will be discussed in the next section.

3.3.2 Influence of fast thermal cycling

In practical applications, fast thermal cycling (FTC) and electromigration (EM) stresses in multilevel interconnects used in power IC's always appear in a combination. The dominant failure can be due to either FTC or EM, depending on operating conditions but it also can be a combination of the two mechanisms. In this work, we study the interaction of the two stresses by applying sequentially FTC and EM stresses. The failure mechanism induced by FTC stress has been found to be a short circuit due to the cracking of the ILD [8] and the dominant failure induced by EM tests in this study is also a short circuit but due to an extrusion. Therefore, it has been predicted (and will be shown later experimentally) that the FTC stress affects the EM lifetime. In this experiment, the devices were first subjected to FTC stress as preconditioning with different conditions as shown in Table 3.2 and subsequently to an EM test with condition, E2 ($J=25mA/\mu m^2$ and $T=150^oC$).

Table 3.2. *Conditions for pre-stress with fact thermal cycling*

Name	t[hrs]	$\Delta T[^oC]$	$T_{min}[^oC]$	f[Hz]	Duty Cycle [%]
Fresh	-	-	-	-	-
F1	16	160	46	10	10
F1'	16	160	65	10	20
F2	32	160	46	10	10
F3	4	200	46	10	10
F4	8	200	46	10	10

Virgin devices were also subjected to the same EM test for comparison. Only the extrusion failure mode was monitored. Devices with package type B were subjected to pre-stressing with all conditions as shown in Table 3.2. For

comparison, type A received only a subset of these. The results of all the EM tests (on virgin as well as pre-stressed devices) are summarized in Table 3.3. It has been recognized that the mechanical stress and strain from the plastic package can cause parametric shifts and physical damage to passivation and metallization layers. Edward et al. have extensively studied the generation of mechanical stress from a plastic package [16]. They show that the moulding compounds and die-attach materials play an important role in the generation of mechanical stress, and can cause a compressive stress and a stress gradient on the silicon die, respectively. These stresses can cause cracks in the passivation layers or transfer of the stress to the metal layers. A significant amount of experimental data has been collected in this area [16-18]. Apparently, package stress can affect the electromigration performance. The effect of mechanical stresses on the EM lifetime already reported in literature [19]. With these in mind, the results of EM tests with condition E2 on virgin devices encapsulated in packages type A and type B are first compared. The lifetime distributions are shown in Figure 3.12, and the MTF and slope, β were extracted (see Table 3.3). It can be seen that the MTF of the package type A is larger than that of the package type B. The slope is only slightly different so that the failure mechanism is supposed to be the same. This observation implies that the electromigration with the extrusion failure mechanism is slightly influenced by the package type. There are two possible explanations for the difference of the EM lifetime between the two packages:

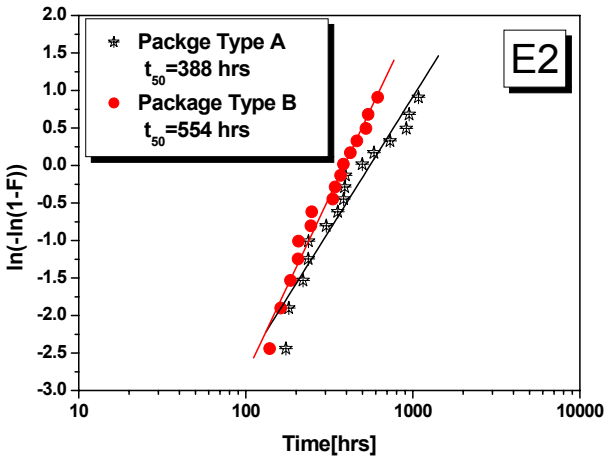


Figure 3.12. *Failure probability plots for electromigration tests at a current stress of 25mA/μm² and temperature of 150°C for packages type A and B.*

Table 3.3. *EM results with FTC as pre-stress*

FTC	EM	Package Type **A**		Package Type **B**	
Pre-Stress	Sub-Test	MTF [hrs]	β	MTF [hrs]	β
Fresh	E2	388	1.8	554	1.6
F1	E2	275	1.5	428	1.5
F1'	E2	326	1.9	473	2.3
F2	E2	*	*	315	2.2
F3	E2	*	*	475	1.5
F5	E2	*	*	405	1.2

(***** *The tests are not necessary*)

(i) the difference in thermal resistance of the two packages can result in a difference in local heating, which can lead to temperature gradients; (ii) the use of different die-attachment materials and moulding compounds, which have different thermal expansion coefficients and mechanical properties can result in the difference in thermal stress at the EM test temperature. It is known that the package type B has a lower thermal resistance than the package type A. This means that the package type B dissipates the heat better than package type A so that the metal lines in package type A are hotter and are expected to have larger gradients in temperature than in the package type B. We have carried out an experiment following EIA/JESD63 of JEDEC-Standard [20] to estimate the Joule heating from devices with package types A and B. It turns out that there is no difference in increase of temperature due to the Joule heating for the two devices and their Joule heating temperature increases are all about 10^{o}C so that the first assumption cannot be responsible for the observed difference in the EM lifetime. The second assumption (ii) could be the main reason for the difference in the EM lifetime of the two packages. The thermal stress at the EM test temperature of package type A (used polymer die-attachment) is higher than that of package type B (used solder die-attachment). Because the solder die-attachment material used in package type B has thermal expansion coefficient (TEC) closer to the lead frame and the silicon chip compared to polymer die-attachment used in package type A. On the other hand, the use of solder die-attachment produces a better uniform distribution of the compressive stress on the die surface. The use of a moulding compound with lower stress can result in a less compressive stress due to a buckle downward of the plastic [16]. This implies that there is more degradation in the layers of devices with the

package type A than type B as stored at EM temperature. These are just preliminary explanations. Further investigation of the effect of plastic package on this EM failure should be done for the reliable explanations. However, it is not an aim of this study. In view of the possible differences per package, it is important to point out that the effect of the FTC on the EM lifetime should be characterized using one type of plastic package for comparison.

The results of the EM tests in Table 3.3 show that by introducing FTC as preconditioning, the EM lifetime is significantly reduced. Apparently, FTC can cause damages to the stressed line (voids-induced) and/or to the ILD (micro-cracking or crack-induced). Voids would result in a local high current density that enhances the EM, whereas a crack (or micro-crack) would result in a decrease of the facture resistance of the ILD, shortening the time for the stress induced by the EM to exceed its fracture resistance. Consequently, the EM lifetime is reduced. Like other annealing treatment. FTC will also affect other metallization properties such as Cu dissolution, diffusion and precipitation and Al crystal defect annealing. Therefore, the EM resistance of the metal line could also be improved after the preconditioning.

However, we did not observe any increases of the EM lifetime from our experiments.

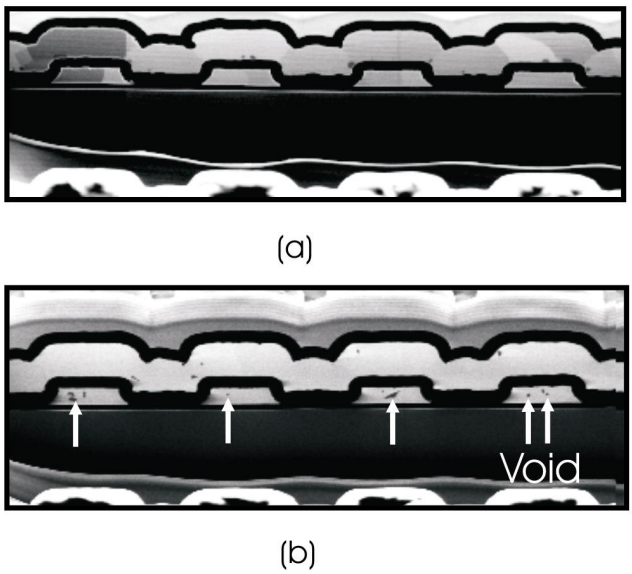


Figure 3.13. *FIB cross-section of test structure:* ***(a)*** *showing no void on the metal line of fresh device,* ***(b)*** *showing voids on the metal line after a few hours of fast thermal cycling stress.*

Apparently, the currently employed annealing process does already result in maximum EM resistance. Like the conventional thermal cycling stress, FTC can also induce voids in the metal line as shown in Figure 3.13b. The voids were observed on the cross-section (by FIB) of the metal line after few hours with FTC stress, but not on the cross-section of the virgin metal line (see Figure 3.13a). The introduction of voids by the thermal cycling has been extensively studied in literature [20,21]. It was shown that the voids nucleation rate depends on the thermal cycling condition such as temperature range, number of cycles, and cycling frequency. This can imply that the reduction of the EM lifetime strongly depends on the FTC conditions.

In Figure 3.14, the reduction fraction of the EM lifetime is shown as a function of the pre-stress time (length of FTC pre-stressing) for two pre-stress conditions. Within the boundaries of this experiment, it is seen that the longer the FTC pre-stress, or the higher the temperature swing, the more reduction in EM is obtained. As reported in the previous publication [8], a FTC stress with a higher ΔT can result in an early failure due to cracking of the ILD. This indicates that if one wants to accelerate EM, FTC pre-stressing with low ΔT and long time is recommended. When we make a particular comparison of the results of the EM tests on the devices (package type A and type B) which were pre-stressed with F1 (ΔT =160°C, T_{min}=46°C, t=16hrs) and F1' (ΔT =160°C, T_{min}=65°C, t=16hrs), we observe that the reduction in the EM lifetime depends on the T_{min} and T_{max}. The reductions in the EM lifetime as a function of T_{min} are plotted in Figure 3.15.

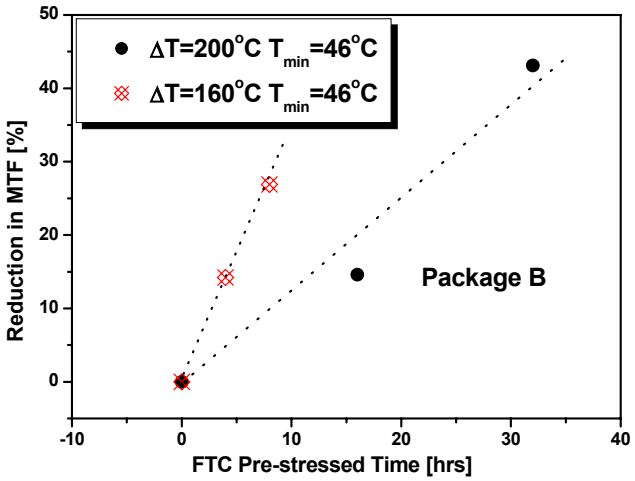


Figure 3.14. *The reduction in the EM lifetime as a function of the pre-stress time.*

It can be seen that the reduction in the EM lifetime increases with increasing T_{min}. This was observed to be the same for the two packages. As discussed above, the FTC can accelerate the EM by the two manners: (i) stress voiding induced in the metal line; (ii) crack (micro-cracks)-induced in the ILD.

When the T_{min} increases the average temperature increases. This may result in an increase of the void density, resulting in an enhanced EM. The reliability tests with the FTC presented in chapter 2 showed that the FTC stress with the same ΔT and higher T_{min} resulted in a longer FTC lifetime (note that the failure mechanism is the cracking of the ILD). This indicates that fewer or smaller cracks (or micro-cracks) are induced during an FTC stress with a higher T_{min}. As we see an enhanced EM when applying an FTC stress at higher T_{min}, a higher void density or more cracks are expected, which is in line with the void growth scenario. Apparently, the stress-voiding manner is dominant in the acceleration of the EM because the ΔT is probably too small to cause the crack or micro-crack in the ILD.

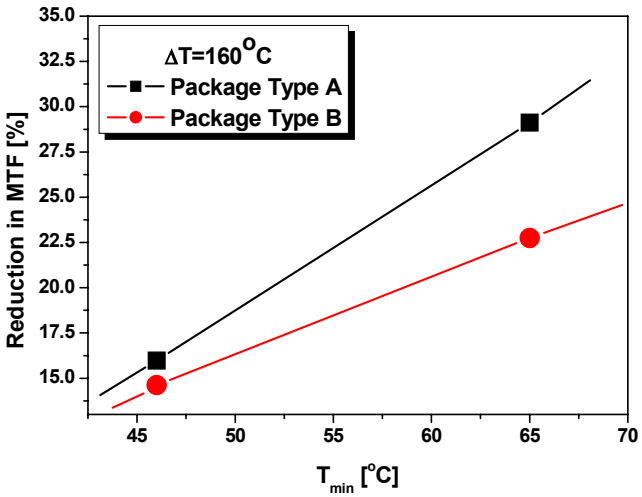


Figure 3.15. *The reduction in the EM lifetime as function of the T_{min} of the fast thermal cycling.*

3.4 Conclusions

Electromigration-induced failure by interlayer extrusion in multilevel interconnects has been investigated. The effect of fast thermal cycling on the electromigration lifetime has been characterized. Interlayer extrusion results in a short circuit between the two metal levels before a resistance increase is

observed. The extrusions mostly happen away from the anode, confirmed by 2D electromigration simulation results in combination with a no-cracking condition analysis and the results of failure analysis. The electromigration-induced interlayer extrusion failure mode appears to be slightly influenced by plastic package type in our case but to extent by the fast thermal cycling pre-stressing. Pre-stressing with fast thermal cycling reduces the electromigration lifetime significantly. The reduction in the electromigration lifetime depends on the cycling temperature range as well as the minimum temperature. The reduction increases with increasing the minimum temperature.

This work has demonstrated a potential failure mode in multilevel interconnects used in e.g. power ICs where the combination of fast thermal cycling and electromigration can result in early failure due to extrusion induced short circuits. This implies that the effect of fast thermal cycling on the electromigration performance should be taken into account when defining electromigration design rules of power IC metallization. An additional observation is that low-k dielectrics are less able to constrain the distortion of interconnects in response to the stresses built-up by electromigration and thermal cycling, as compared to the conventional dielectrics SiO_2 and Si_3N_4. Therefore, this study implies another challenge for the already challenging advanced interconnects using low-k materials.

3.5 References

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CHAPTER 4

Electrothermomigration on Power IC Metallizations

CONTENTS

Metal migration driven by electron flow and temperature gradients is a major concern for power IC (integrated circuit) reliability, especially in advanced ICs where there is an increased density of the integrated power components and power dissipation. This chapter presents studies on the electrothermomigration failure mechanism that can occur in power IC metallization where hot spots from active devices can induce a large temperature gradient in the conductors. Temperature gradients can lead to thermomigration but more important, they act as sources of electromigration flux divergence in the metal line. For this work, a special test chip was designed, which can be used to perform electromigration tests under uniform temperature or in the presence of a temperature gradient. A matrix of experimental conditions has been studied. A model to explain the failure mechanism of electromigration under a temperature gradient stress has been explored, and is consistent with observations from failure analysis. This work demonstrates the importance of temperature gradients, which can make the electromigration lifetime much shorter compared to the uniform temperature case. Therefore, the results from conventional electromigration tests would not be valid for extrapolations of the power IC lifetimes to the use condition. Applications for design rules and material characterization for power IC metallization are discussed.

4.1 Introduction

Multilevel interconnects used in power integrated circuits (ICs) contain metal lines with very large dimensions that connect outputs and power devices. Their width and thickness can be several micrometers. During the operation of power ICs, these metal lines are subjected not only to a high current density but also to a temperature gradient, which is generated by non-uniform Joule heating as well as dissipation from the active power elements in underlying silicon. It has been reported that the wider metal lines are already more susceptible to electromigration (EM) than narrow ones [1]. This is due to the presence of microstructures with triple-points in the wider metal line having higher flux divergences than in the narrow metal line with the bamboo microstructures. For advanced silicon technologies, there is a rapid increase in the density of the integrated power components and the accompanying power dissipation that causes a remarkable temperature gradient, which can enhance EM [2] and induce thermomigration (TM) [3]. For these reasons, the role of temperature gradients in EM and TM, which is commonly accepted to be negligible in normal interconnects, will play a role in the larger power metal lines. A full understanding of these issues is very important to build a good EM design rule for power IC's, and the lifetime is accordingly optimized. However, there is very limited data about electrothermomigration available in literature. In early studies, the temperature gradient dependence of the electromigration failures has been confirmed by Schwarzenberger et al [2] and Lloyd and Shatzkes [4]. They demonstrated that the temperature gradients act as sources of atom flux divergence in the metal line during the EM process. Temperature gradients can also lead to TM, but usually, its driving force is much smaller than that of EM. This is the main reason why the role of TM in EM has not attracted much attention in previous work. Recently, Ru [5] has reported that TM is the leading driving force for instability of the EM-induced mass transport in interconnect lines, and it plays a significant role in the EM failure of interconnect lines. This theoretical prediction seems to qualitatively agree with a previous experimental study [6]. In this chapter, an investigation of electrothermomigration in large and thick metal lines, which are based on the metallization process of industrial power IC's to simulate the combined thermal and electrical effects in power ICs, will be presented. In the following sections the experimental details, including the description of the special EM test structure, the test set-up and the calibrations for the on-

chip temperature sensor will be presented. Thereafter, results of the electrothermomigration experiment will be given. Then an application of this experimental technique for power IC metallization characterization will be demonstrated. Application of the results for reliability predictions of power IC metallization is discussed in the conclusion section of this chapter.

4.2 Experimental details

In this study, a special test chip for electrothermomigration experiments is described. A standard EM test structure is integrated with several heater elements (HE) and temperature sensors (TS), which can be used to impose and measure temperature, respectively. The test set-up and calibrations for the temperature sensors are also represented.

4.2.1 Description of the test chip[7]

The test structure schematically shown in Figure 4.1 has been designed with a conventional single metal level for standard EM testing [8]. Besides, it contains three heater elements (HE) and four on-chip temperature sensors (TS). The temperature sensors are p/n diodes, just below the die surface, which are isolated by a 0.5μm SiO_2 layer.

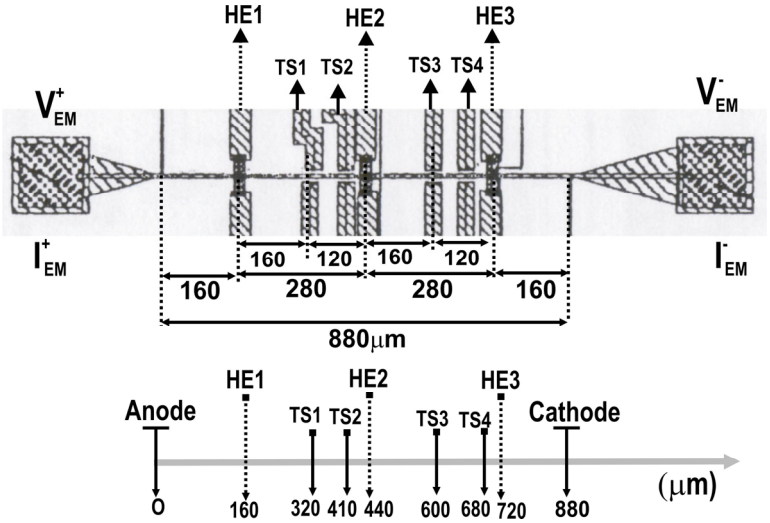

Figure 4.1. *Schematic diagram of the test structure; TS is the temperature sensor (intergraded diode); HE is the heater element (poly-Si line); the showing dimensions are all in μm; the vertical co-ordinates of heater elements and temperature sensors are shown.*

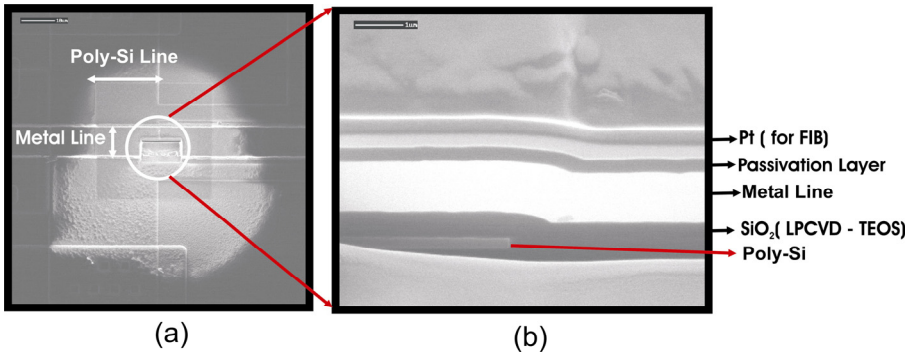

Figure 4.2. *SEM images: (a) the position of the cross-section; (b) the cross-section by FIB showing the different layers.*

The heater elements are poly-Si lines, and they were realized on three positions as shown in Figure 4.1 (near cathode, anode, and in the middle of the metal line). Between the heater elements, there are two diodes, which are located at short and long distance (see Figure 4.1) to the heater elements to measure temperature and estimate the temperature gradients. Before deposition of the metal layer, the die surface is isolated by a 0.4µm SiO_2 layer, which is deposited by LPCVD (Low Pressure Chemical Vapor Deposition) using TEOS (Tetraethylorthosilicate). The aim of the use of TEOS is to improve the step coverage of the metal line over the poly-Si lines (heater elements). At the end, a Si_3N_4 passivation layer with the thickness of 1.8µm was deposited by PECVD (Plasma Enhanced Chemical Vapor Deposition). Figure 4.2 shows the cross-section made by FIB (Focused Ion Beam) at the edge of poly-Si line to view the step coverage of the metal line and a stack of layers of test structure. A standard industrial Al alloy AlSi(1%)Cu(0.04%) metallization was used in this test structure. The thickness and the width are 2.5µm and 10µm, respectively. The length of the metal line and the positions of heater elements and temperature sensors can be found in Figure 4.1. The test structure was mounted in a 24 pins ceramic package.

4.2.2 Description of the test set-up

The test set-up as shown in Figure 4.3 has been realized for this study in our lab. It can be seen that the test set-up consists of three blocks. Block (I) is a DC current source to force a constant current though the heater elements to impose a temperature gradient. Block (II) is used for EM measurement. In this block, we have employed a SourceMeter Keithley 2420.

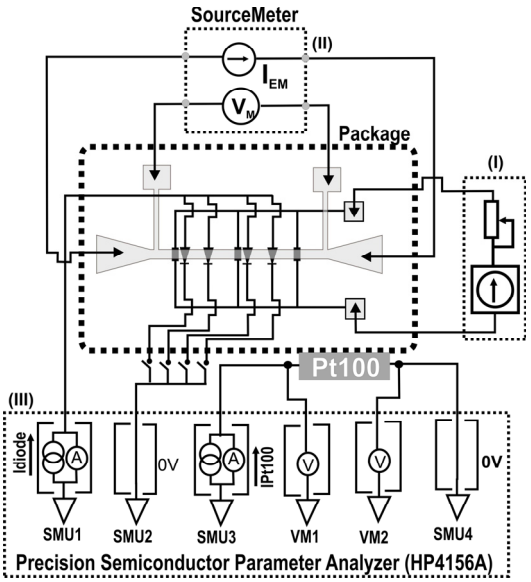

Figure 4.3. *The set-up used in this work: block (I) is a current source connected to heater elements; block (II) is a sourcemeter for electromigration test; block (III) is the precision semiconductor parameter analyzer for temperature measurements with integrated diodes and temperature sensor Pt100.*

It can be used to force a current from 500pA to 3A with a high stability, and the voltage is measured with an accuracy of 5-1/2 digit resolution [9]. These accuracies agree with the standard as proposed in [8]. Block (III) is a scheme to measure the temperature inside the chip with the on-chip temperature sensors (integrated diodes) and the package temperature with an external temperature sensor (Pt100) on top of the package, using a HP4156A (precision semiconductor parameter analyzer). This equipment can supply output current resolution from 100fA to 10μA, depending on the output value, and it can measure the voltage with resolution from 2μV to 200μV, depending on the measurement range. In this experiment, a Heraeus Intruments oven with a Shimaden Co. LTD. FP21 Series programmable controller is used. It can keep the temperature stable within tenths of a degree.

4.2.3 Temperature sensor calibrations

The use of the diode as a temperature sensor was previously discussed in detail in the section 2.2.3 of chapter 2. However, the diode used in this study was fabricated in a different process. Therefore, the calibration of the diode therefore needs to be done again.

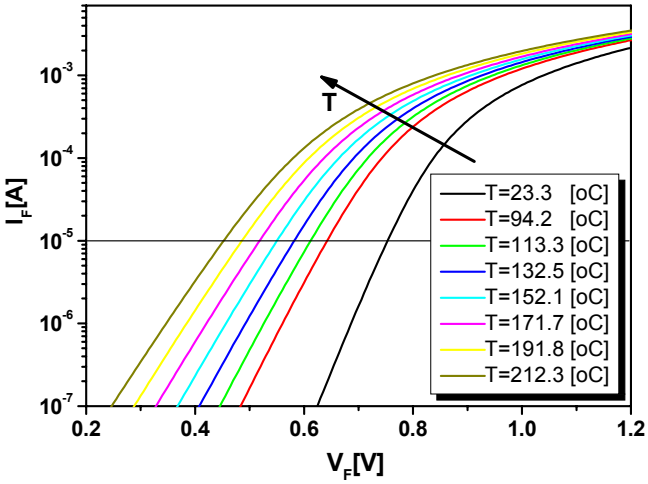

Figure 4.4. *Current versus voltage characteristics of the diode used in this study (I_F-V_F) over a range of temperatures.*

The diode characteristics measured at different temperatures are shown in Figure 4.4. As discussed in chapter 2, the simplified form of Shockley's relation, which is valid only in the linear portions of diode characteristic, is used to determine temperature. As can be seen in Figure 4.4, a current value of 10μA is a well-chosen value to operate the diode in the linear portion for temperature measurement during testing. The calibration steps are conducted in an oven because it is easy to set and control the temperature.

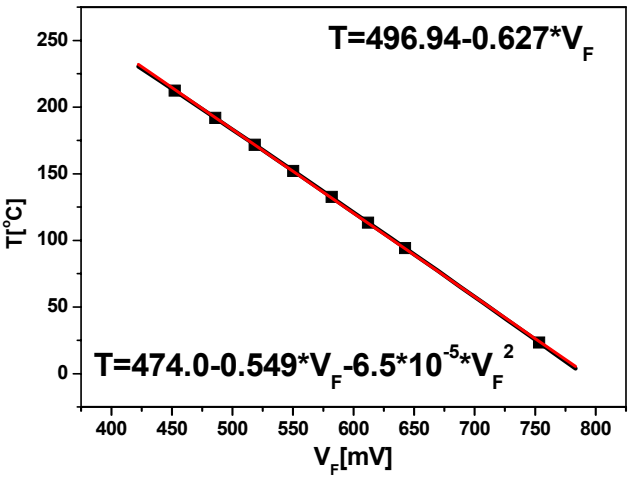

Figure 4.5. *Calibration data for the diode (at 10mA current) fitted to a liner and second order curves.*

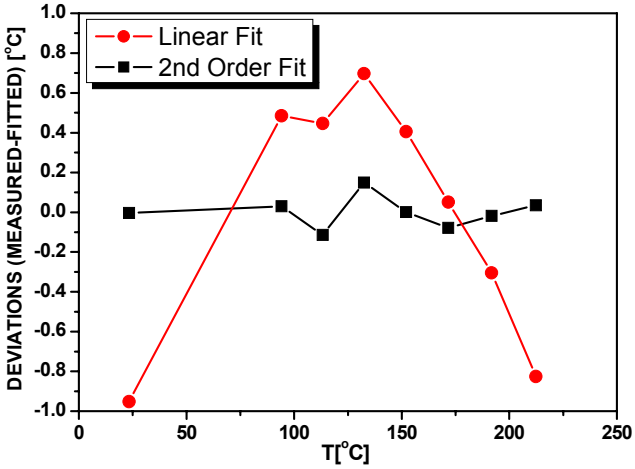

Figure 4.6. *Deviations between measured and fit data in cases of linear and second fits with different temperatures.*

During a calibration step, the temperature of the oven is monitored by the temperature sensor Pt100 mounted on the top center of the package. At the same time, the diode voltage is also monitored. At steady state (showing a variation of about 0.1°C on the temperature sensor Pt100), the diode voltage and the temperature indicated by the Pt100 were recorded. Next, the oven was set to a higher temperature, and the measurements were repeated as above. The results of the calibrations at room temperature (23°C) and over a temperature range from 94°C to 212°C are shown in Figure 4.5. It also shows the linear and second order fits to the data. The deviations between measured data and the fitted line are shown in Figure 4.6. In case of linear fit, the maximum deviation (measured value-fitted value) is about 1°C, and measured temperature is carried out beyond the calibration range that can result in a much higher deviation (see Figure 4.6). This means that the measurement beyond calibration range results in a large error. In case of second order fit, the maximum deviation is about the 0.15°C. Therefore, to determine the temperature beyond the calibration range, the second order fit is used.

4.3 Results of electrothermomigration experiments

In this section, the test structure as shown in Figure 4.1 is used to perform EM tests in uniform temperatures and in the presence of a temperature gradient for comparison. Different current densities and temperature gradient conditions are also studied. The modelling and theoretical model for this failure mechanism will also discuss.

4.3.1 Effect of temperature gradient on current exponent

Conventional EM tests were performed at ambient temperature T=202°C and under different current densities J=8, 10, and 12mA/μm^2. Other EM tests were also done at the same current densities but in the presence of a temperature gradient for comparison. The temperature gradient conditioning is carried out as follows; the oven temperature (T_{oven}) is first controlled at 152°C. Actually, this temperature is measured by the temperature sensor Pt100 mounted on the package, and it can be considered as ambient temperature at this moment. When the oven temperature is stable, a temperature gradient is imposed using the on-chip heater elements. The temperatures at the heater elements (T_{HE}) are measured by the on-chip temperature sensors and controlled so that these temperatures are at 202°C. Approximately, these temperatures can be considered as the temperatures of the hot spots (at the heater elements) because the temperature sensors were laid out very near the heater elements (from 15-20μm). Note that during the time that a temperature gradient is imposed, the package is heated up and becomes hotter than the ambient temperature. This means that the package temperature (T_{pack}) is higher than the oven temperature. Hence, this package temperature is considered as ambient instead of the oven temperature. The relationship between the package temperature and the hot-spot temperature before and after imposing a temperature gradient is shown in Figure 4.7.

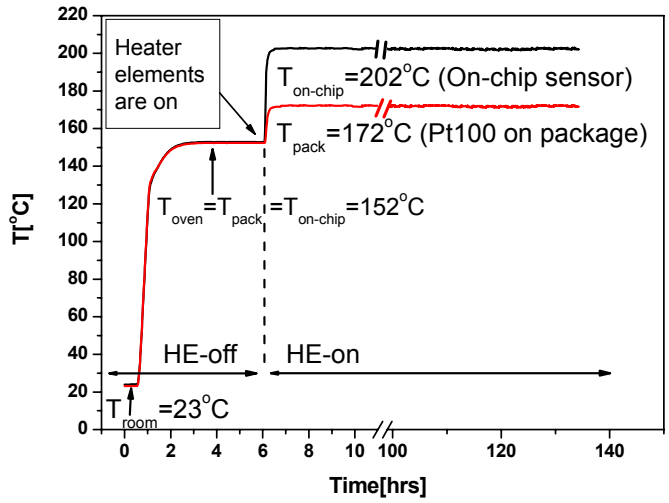

Figure 4.7. *Temperatures on the package and inside the chip are measured by the temperature sensor Pt100 and diode temperature sensor before and after locally heating for EM test in the presence of a temperature gradient.*

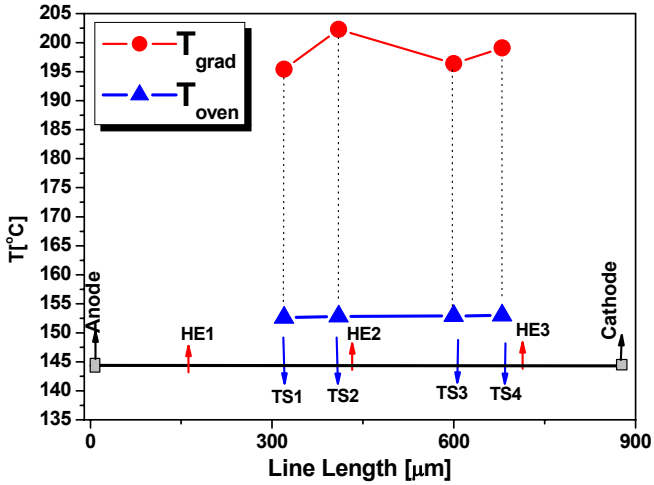

Figure 4.8. *The temperatures measured by the temperature sensor (TS) at different locations before and after an imposed temperature gradient.*

The temperatures at different locations measured by the on-chip temperature sensors before and after imposing a temperature gradient are given in Figure 4.8. This is not yet representative of the temperature gradient profile, because the positions of on-chip temperature sensors are not yet optimized to measure the temperature of the locations along the metal line where the temperature is lowest. The importance of this measurement is that the temperatures at the hot spots and other locations were determined to confirm the presence of a temperature gradient along the length of metal line and to control the hot-spot temperatures for EM test purposes. Approximately, a temperature gradient can be calculated by equation:

$$\nabla T = \frac{T_H - T_L}{X_H - X_L} \tag{4.1}$$

Where, T_H and T_L are the high and low temperature, respectively, and X_H and X_L are the co-ordinates of the high and low temperatures along length of the metal line. The maximum temperature gradient ∇T_{max} can be calculated by taking $T_H=T_{HE}=202^oC$, $T_L=T_{pack}=172^oC$ (see Figure 4.7), and X_H-$X_L=160\mu m$ (see Figure 4.1), and ∇T_{max} is found about $0.2^oC/\mu m$. It can be recognized that the temperature gradients in the metal line are definitely lower than this temperature gradient value (∇T_{max}). Because there are not any locations along the metal line with the temperature, which is lower than the package temperature T_{pack}. When the imposed temperature gradient is stable, the EM current is switched on for testing.

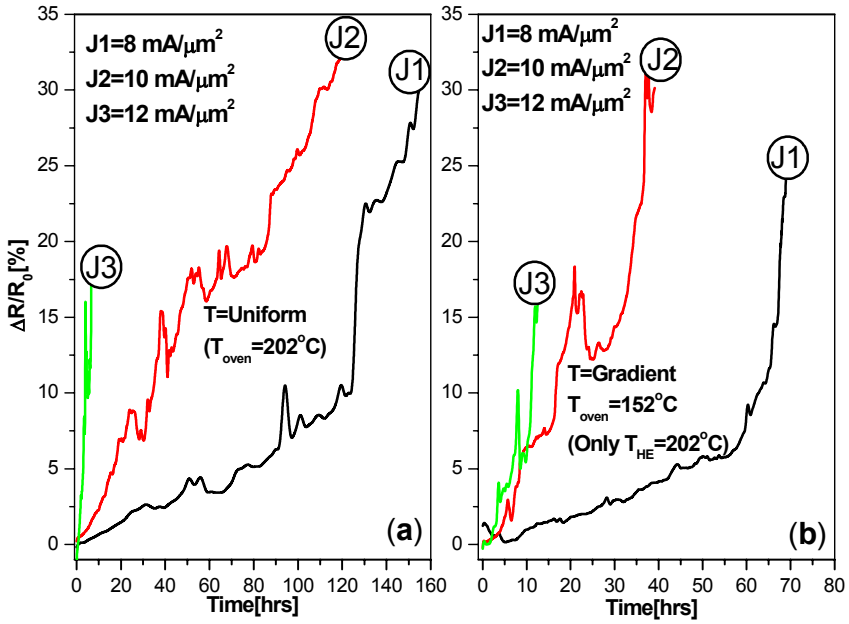

Figure 4.9. *Relative resistance change for: (a) EM- test at uniform temperature T_{oven}=202°C (b) EM-test with applied temperature gradient, T_{oven}=152°C, T_{HE}=202°C. Note the different time axes.*

Typical results of the relative resistance change (RRC) versus time observed from the EM tests under uniform temperature and the presence of a temperature gradient are shown Figure 4.9(a) and (b), respectively. The current densities J=8, 10, 12mA/μm^2 were used in these tests. It can be seen that in both cases, a higher current density results in a higher rate of resistance increase of the metal line. Interestingly, the resistance increases faster in the presence of a temperature gradient than in a uniform temperature. The results of time-to-failure (TTF) as extracted from the RRC curves are shown in Table 4.1. A failure criterion of 15% resistance increase was used. It has been observed that the EM lifetimes are always shorter in the presence of a temperature gradient than in a uniform temperature. As mentioned above, in these experiments, the stress temperature is strictly controlled.

Table 4.1. *TTF results under uniform temperature and temperature gradient.*

J[mA/μm^2]	TTF [hrs] Uniform temperature	TTF [hrs] Temperature gradient
8	125.8	67.1
10	46.6	19.8
12	11.8	3.9

In case of the temperature gradient, only temperatures at the hot spots (heater elements) reach 202°C, the other locations are at temperature lower than 202°C so that the average temperature of the metal line is properly lower than 202°C. This is to indicate that the EM lifetime reductions in case of temperature gradients are not due to any higher temperatures because EM tests under uniform temperature were performed under ambient temperature of 202°C. Apparently, a temperature gradient can cause TM (atoms diffuse from the hot to cold locations). It has been reported in the literature [3] that TM can enhance EM when the driving force sign of temperature gradient is the same as the driving force of the electron current. On the contrary, TM can delay EM. In this experiment, there is no polarization of the temperature gradient along the length of the metal line (not hot at anode and cool at cathode, or the other way around). There are just few hot spots along the length of the metal line. We always observe that the EM lifetimes in the presence of a temperature gradient are significantly shorter than in uniform temperature (see table 4.1). It can be seen that this temperature gradient is not yet high enough (lower than 0.2°C/μm) to induce a significant TM (will be explained later) for those lifetime reductions. A strong effect of temperature gradient on the EM lifetime is supposed to be a better explanation for that because temperature gradient can induce higher flux divergences and is the cause of the lifetime reductions. This observation is in qualitative agreement with a recent theoretical model [5]. This report showed that a low TM could play a significant role in the EM-induced failures.

Joule heating during EM testing can also result in a temperature gradient itself that can induce the EM failure with a different failure mechanism [10]. With this in mind, the Joule heating needs to be estimated for our experiment. To do so, the resistance of the metal line was measured at different temperatures to find its thermal resistance coefficient. Figure 4.10 presents a plot of resistance versus temperature taking equation:

$$R_T = R(T_{ref}) + S(T - T_{ref}) \tag{4.2}$$

Where, S is slope of the resistance versus temperature plot and $R(T_{ref})$ is the resistance of the test line at a reference temperature T_{ref}. We found the slope S= 0.006Ω/°C. The Joule heating can be calculated as follows:

$$\Delta T_{Joule} = \frac{R_H - R(T_H)}{S} \tag{4.3}$$

Where $R_H(T_H)$ is the resistance measured at the stress temperature T_H with a low current, and R_H is the resistance measured at the stress temperature and stress current (for EM tests). In Figure 4.11, we plot ΔT_{joule} versus current density for this test structure held at an oven temperature of 152°C and current density ranging from 6 to 16mA/μm^2. We assume that the median-time-to-failure (MTF) for EM follows the Black equation [11] as follows:

$$MTF = Aj^{-n} \exp\left(\frac{E_a}{kT}\right) \tag{4.4}$$

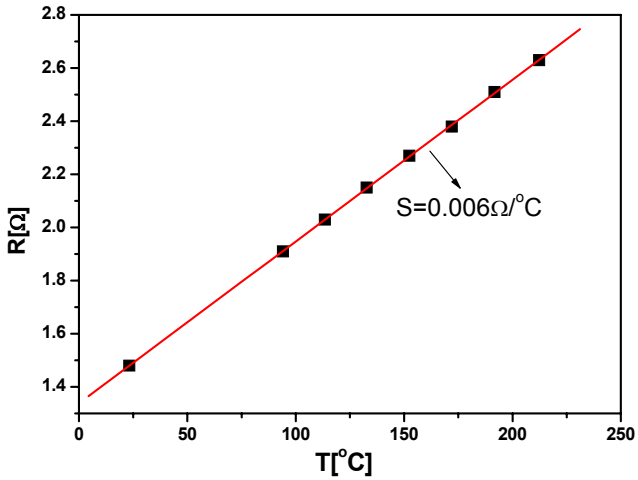

Figure 4.10. *Resistance versus temperature for metal line of the test structure.*

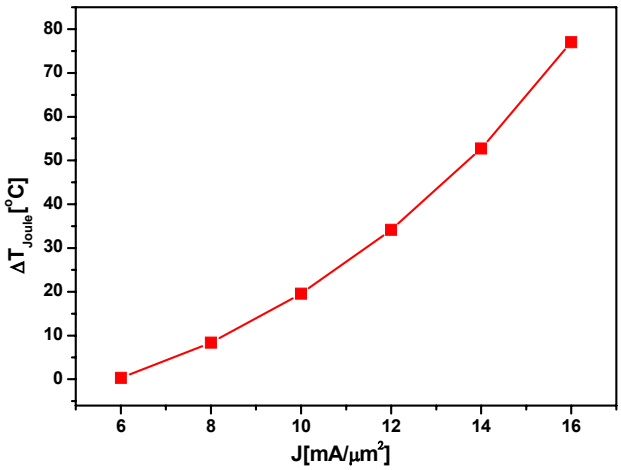

Figure 4.11. *The temperature increases due to the Joule heating.*

Where, j is the current density, E_a is the activation energy, n and A are constant, and k is Boltzman's constant, T is the temperature in Kelvin. To find the correct current exponent value n, the Joule heating ΔT_{Joule} must be added in the equation (4.4):

$$MTF = Aj^{-n} \exp\left(\frac{E_a}{k[T + \Delta T_{Joule}]}\right) \tag{4.5}$$

It can be seen that to make the Joule heating correction, the E_a value needs to be estimated in advance. As mentioned above, the metal line used in this test structure was fabricated with a standard process at a fab following a design manual. Therefore, the E_a was already known to have a value of 0.65eV from previous experiments. Another thing to mention is that in case of temperature gradient, the average temperature, which is an average of the temperatures measured by the on-chip temperature sensor, is used to represent the metal line temperature. In Figure 4.12, we plot $\ln(TTF)-E_a/k(T+\Delta T_{Joule})$ versus ln(J), and the linear fit results are shown in the same figure. The calculated n values after the Joule heating correction are 2.9 and 4.3 for the EM tests under uniform temperature and temperature gradient, respectively. The n value in case of uniform temperature is quite comparable with the reported values in the literature [11,13] as well as with the n value from the design manual (n=2.3). However, the n value in case of temperature gradient seems far too high.

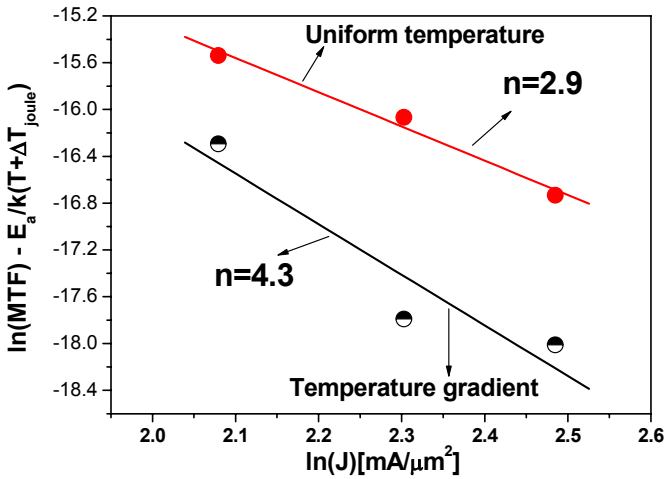

Figure 4.12. *Fitting of TTF data with the correction of Joule heating at three different current densities for both temperature conditions.*

This indicates an effect of temperature gradient on the current exponent for failure. This observation is important, and design rules for power ICs should consider this because the use of an erroneous value for n could lead to errors in extrapolation of the lifetime at the use condition. However, a large number of devices need to be tested to establish a better design rule.

4.3.2 Impact of temperature gradient on electromigration

This experiment explores the acceleration level of a temperature gradient to the electromigration failure. To do so, EM test in the presence of a temperature gradient under the current density of $10mA/\mu m^2$ is repeated with different temperature gradient conditions. The different temperature gradient conditions are done as follows; the oven temperatures are controlled at 127°C, 152°C, and 177°C, and then the temperatures at heater elements are controlled so that they are all 202°C. The temperatures measured by the temperature sensors are shown Figure 4.13, for all three cases. Table 4.2 summaries different temperature aspects such as T_{oven}(oven temperature), T_{pack}(package temperature during imposing a temperature gradient), T_{HE}(temperature of the hot spot), T_{avg}(the average temperature of the metal line calculated by making the average of temperatures measuring by the on-chip temperature sensors, and maximum temperature gradients ∇T_{max}. Typical RRC results of the EM tests with stress current density of $10mA/\mu m^2$ under these temperature gradient conditions are shown in Figure 4.14. A slight increase of ∇T results in a high rate of the relative resistance change (RRC) increase, while the average temperatures of metal line under tests are not much different. This means the EM lifetimes are significantly decreased as given in Table 4.2.

Table 4.2. *The different temperature gradient conditions are imposed during EM tests.*

Parameters	Uniform Temp.	Tgrad1	Tgrad2	Tgrad3
T_{oven}[°C]	202	127	152	177
T_{pack}[°C]	202	157	172	187
T_{HE}[°C]	202	202	202	202
T_{avag}[°C]	202	196	198	200
∇T_{max}[°C/μm]	-	0.28	0.19	0.09
TTF[hrs]	46.6	4.3	19.8	41.8

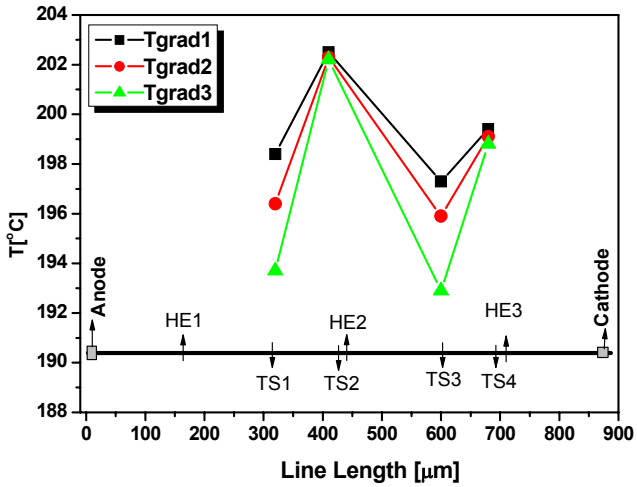

Figure 4.13. *The temperatures measured by the temperature sensor (TS) at different locations from different temperature gradient conditions.*

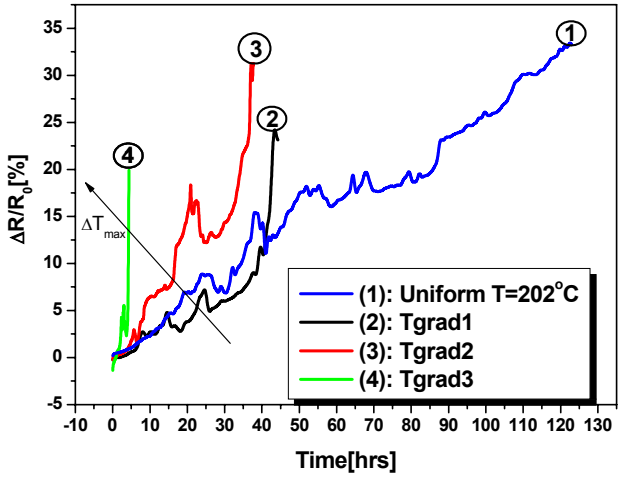

Figure 4.14. *The relative resistance change at different temperature gradient conditions and uniform temperature T=202°C, and J=10mA/μm².*

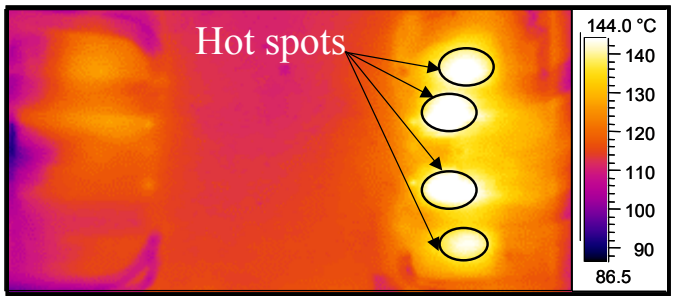

Figure 4.15. *An example of temperature mapping by Infrared Spectroscopy of commercial power IC during operation showing a hot-spot more 20°C hotter than nearby regions [12].*

These temperature gradients are similar to or less severe than those found in commercial power ICs where a hot spot may be more than 20°C hotter than nearby regions as depicted in Figure 4.15 for example [12]. This points out that the EM tests in the presence of a temperature gradient are extremely important in building an EM design rule for power IC metallizations.

4.3.3 Failure mechanism discussion

It is well accepted that the EM failure is caused by vacancy diffusion related mechanisms. There are typically three primary driving forces for vacancy diffusion in the metal line under an applied current: (i) the electrical current (electromigration); (ii) mechanical stress (stressmigration) gradient; (iii) temperature gradient (thermomigration). Based on the model proposed by Clement and Thompson [14], a vacancy flux can be approximated by the following equation:

$$J_v = -D_v\left[\nabla C_v + \frac{C_v}{kT}\left(Z^* e\rho j + \Omega\nabla\sigma - \frac{Q^*}{T}\nabla T\right)\right] \tag{4.6}$$

Where $D_v=D_0\exp(-E_a/kT)$ is the vacancy diffusivity, kT is the thermal energy, Z* is the effective change number, e is the elementary charge, ρ is the resistivity, j is the current density, Ω is the atomic volume, ∇ is the gradient operator, σ is the tensile stress, and Q* is the coefficient of heat flux. As mentioned above, TM has been ignored in recent research, due to the fact that the EM driving force is much larger the TM driving force. Now, we estimate both of these driving forces in our case for a comparison. In these calculations, some parameters are taken from literature: Q*=1eV, and ∇T is taken from our experiment (see Table 4.2), j=10mA/μm^2, Z^*=-10, T=[202+273]K (our experiment), ρ=4μΩcm, we find; the maximum of the TM driving force $F_{TM}(max)= Q^*(\nabla T_{max}/T) \approx 6$eV/cm(because of the use of ∇T_{max}). Actually, the TM driving forces from our experiments are much lower that this value, because the ∇T_{max} was used in this calculation. The EM driving force is calculated by $F_{EM}=Z^*e\rho j=40$eV/cm. These calculations are to point out that the driving force of TM is much smaller than that of EM. Therefore, reductions of the EM lifetime cannot be explained due to an enhancement of pure TM. In early studies [2,4], it was shown that besides the small TM flux, the temperature gradient induces flux divergences [4]. Therefore, EM-induced failures under a temperature gradient can occur with

competition of two mechanisms, which are: (i) flux divergence due to microstructure (grain boundary); (ii) flux divergence due to temperature gradient. With a high temperature gradient in the metal line, the second mechanism can be the dominant mechanism, and failure locations are typically near to the location of maximum temperature gradient, but not exactly at the highest temperature location. Because failure locations are determined by the gradient of atom flux rather than the magnitude of atom flux. With EM under uniform temperature, flux divergence due to microstructure dominates so that the failure locations are randomly distributed. SEM (Scanning-Electron-Microscope) verifications of failure locations of failed samples of EM tests under uniform temperature and temperature gradient are shown Figure 4.16(a) and (b), respectively. Note that only parts of the metal line near heat elements are shown in this figure. We indeed observed that mostly, the failure locations (the circle symbols) by the EM-induced under temperature gradients distribute near the hottest region and on the cathode side of heater elements (the square symbols). This can be understood with the model as shown in Figure 4.17. The equation (4.6) shows that the atom flux (or vacancy flux) is exponentially proportional to the temperature (through D_v).

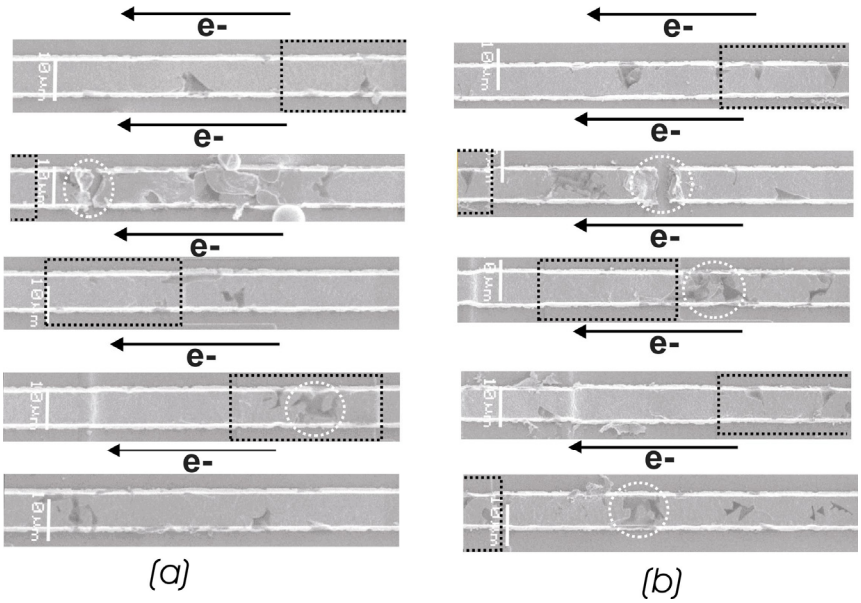

Figure 4.16. *SEM images showing failure locations of EM tests with J=12mA/μm²: (a) in uniform temperature, (b) in the presence of a temperature gradient.*

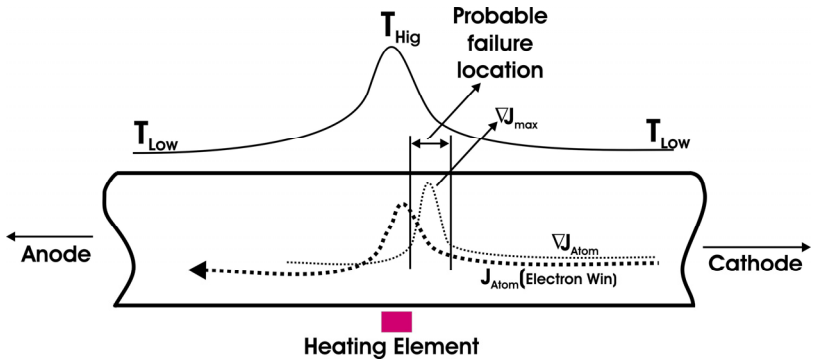

Figure 4.17. *Schematic model indicating likely failure locations in case of EM test under a temperature gradient.*

Therefore, only a small difference in temperature between locations can result in a large difference in atom flux, and cause flux divergence somewhere near heater elements but not exactly at the highest temperature locations.

The discussion above is just a qualitative explanation to understand the effect of the temperature gradient on EM. Recently, Ru has developed a physical model, in which the important parameters such as C_v, T, j and σ are treated under perturbed state in the presence of a temperature gradient to analyze the effect of temperature gradient on EM-induced failure. It is well known that the continuity equation proposed in [15] is usually used to model the EM phenomena of a conductor line. It is expressed as follows;

$$\frac{\partial C_v}{\partial t} - \frac{\partial C_L}{\partial t} = -\nabla J_v \tag{4.7}$$

Where, C_L is the concentration of lattice sites. As the equation (4.6) is used to solve the continuity equation (4.7). The parameters in those equations must be treated as perturbed states as follows [5]:

$$C_v = C_v^o + \Delta C_v(x,t);\ J_v = J_v^o + \Delta J_v(x,t);\ \sigma_v = \sigma_v^o + \Delta\sigma_v(x,t)$$
$$C_L = C_L^o + \Delta C_L(x,t);\ T = T^o + \Delta T(x,t) \tag{4.8}$$

Here the superscript "0" denotes the unperturbed state, and Δ denotes the variations. Other parameters are also in a relatively perturbed state D (diffusion coefficient) and ρ (resistivity of the conductor line). They are dependent on the temperatures as expressed below:

$$D=D^*\exp(-E_a/kT)\ ;\quad \rho=\rho_0[1+\alpha(T-T_{ref})]\ (\alpha>0) \tag{4.9}$$

Where, D^* is a material constant, T_{ref} is the reference temperature, and α is a thermal resistance coefficient.

Ru [5] has analytically solved equation (4.7), using equations (4.6), (4.8), and (4.9). Ru's result shows TM induced failure can be ignored but it could play a significant role in the EM-induced failure of the metal line, in which TM is the leading driving force for instability of EM-induced mass transport in metal line. This observation seems to qualitatively agree with our experimental results.

4.4 Application for rapid characterization of power IC metallization

In this section, the determination of the activation energy in the presence of a temperature gradient is demonstrated, which is a typical application of this model. This is done in the interest of reducing cost for the reliability tests. The time needed to obtain the EM lifetime data under stress condition of low current density and low temperature can be extremely long. As presented above, a temperature gradient can be used to accelerate EM. Therefore, it would be very useful if the activation energy could be obtained from EM test in the presence of a temperature gradient. Even when the actual magnitude of the EM lifetime might not be useful, the temperature dependence obtained by the activation energy might be. There is nothing which indicates that the activation energy for diffusion in the presence of a temperature gradient should be any different from the uniform temperature situation. Therefore, if the failure is due to a diffusion failure mode such as EM, the activation energy in the presence of a temperature gradient should be the same in case of a uniform temperature. A temperature gradient technique for measuring the activation energy for electromigration was already reported in the literature [16]. However, this technique is quite complicated and it is not possible to carry out the test using commercial EM equipment. Below, a special test chip, which can be used to perform EM test in the presence of a temperature gradient with commercial EM test equipment, and preliminary results of characterization of the activation energy is given.

4.4.1 Description of the test chip

Basically, this test structure (see Figure 4.18) is similar with the test structure with three heater elements as previously described in section 4.2.1. The differences are; there are four heater elements and eight temperature sensors, the length line is longer than the previous structure, and especially, the heater elements are connected in series to the metal line so that electrical current

passing through metal line for EM test also passing through the heater elements and a temperature gradient is accordingly imposed. This test chip has more on-chip temperature sensors along the length of the metal line compared to previous once so that the measured average temperature of the metal line is more accurate. This is a very important aspect in the determination of the activation energy. Advantages of this test structure are that it can carry out the EM test with commercial EM test equipment. Therefore, it will enable rapid characterization of different types of metallization to be made, and their suitability for power IC metallization can be examined.

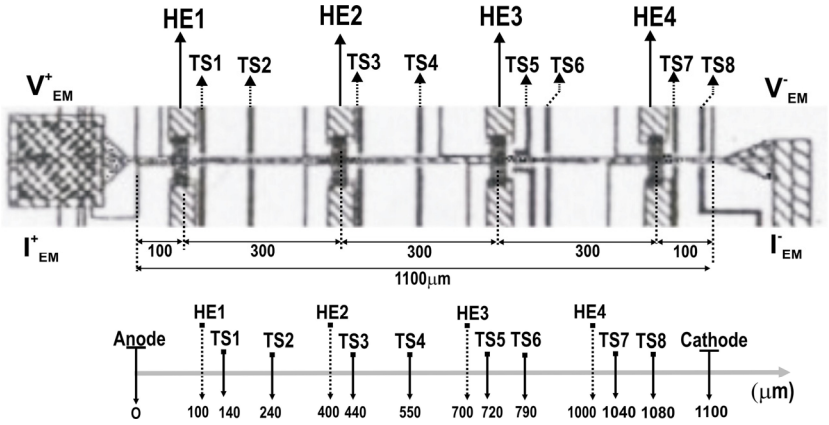

Figure 4.18. *Schematic diagram of the test structure; TS is temperature sensor (intergraded diode); HE is heater element (poly-Si line); the showing dimensions are all in μm; the vertical co-ordinates of heater elements and temperature sensors are shown.*

4.4.2 Preliminary results and discussion

As mentioned above, a current density passed through the metal line for the EM test will also impose a temperature gradient. Therefore, EM test under different current density is also under different temperature gradient conditions. Figure 4.19 shows temperatures imposed by different current densities are measured at different locations using on-chip temperature sensors (TS). A high temperature inside the chip can be achieved with a typical EM stress current (lower than 20mA/μm^2), and a higher current density can result in a steeper temperature gradient as can be seen in Figure 4.20. The difference in temperature between hot spots and other locations can be up to 20°C with a current density of 11mA/μm^2.

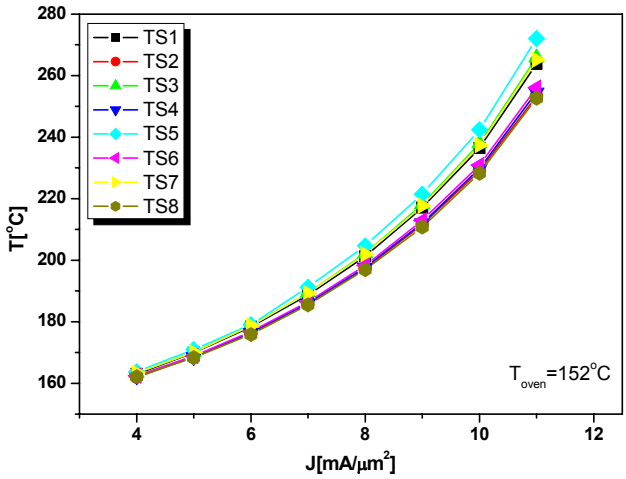

Figure 4.19. *Temperature gradient imposed with different current densities.*

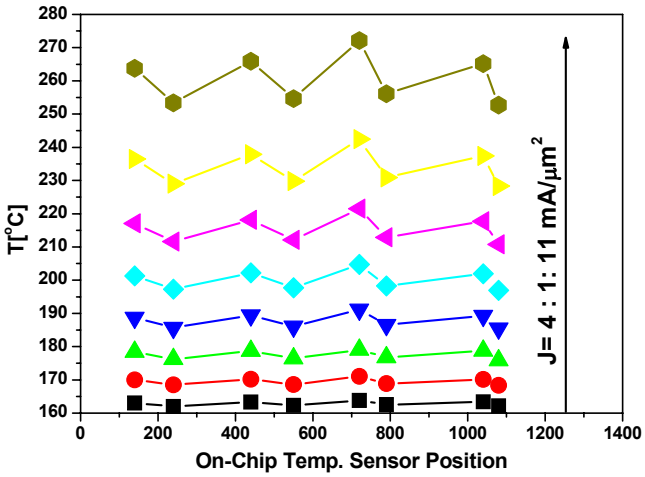

Figure 4.20. *Temperature profiles under different current densities.*

These temperature gradients are somehow comparable with that found in commercial power ICs (see Figure 4.15). This design and method can therefore be used to study in a standard test environment, the effect of temperature gradient on power IC metallization failure mechanisms. An equivalent activation energy can then be derived from the measurements. The test structure as shown in Figure 4.18 is used to perform EM test under a current density of 8mA/μm^2 and different oven temperatures of 172°C, 192°C, and 212°C. The temperature conditions before and after switching on the EM stress current are shown in Figure 4.21.

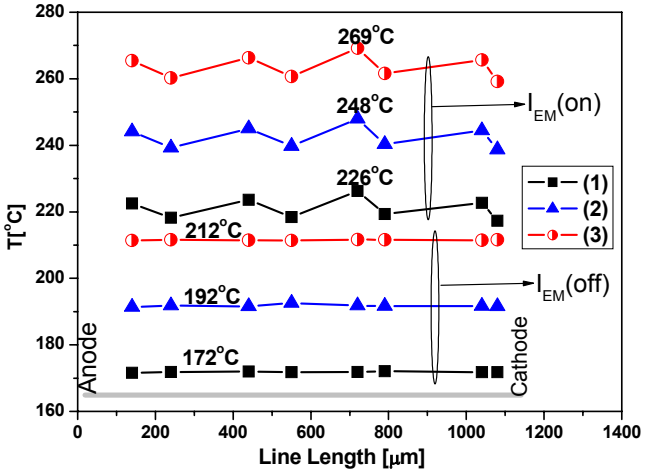

Figure 4.21. *Temperaturesalong metal line before and after switching on of EM stress current, J=8mA/μm2.*

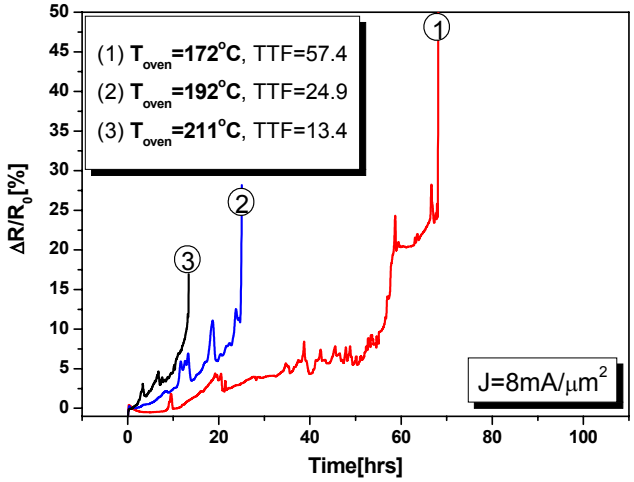

Figure 4.22. *Relative resistance change of metal line at different oven temperatures, and current density of 8mA/μm².*

With this temperature conditioning, temperature gradients for three cases are similar, but the average temperatures of metal line are different. The average temperatures are calculated as the mean of the temperatures measured by temperature sensors. Typical test results of relative resistance change are shown in Figure 4.22. A failure criterion of 15% resistance increase is used to extract the EM lifetime. The lifetimes are plotted as a function of reciprocal temperatures as shown in Figure 4.23, and the activation energy of 0.78eV was found. Note that this experiment is just to demonstrate a typical application of this model.

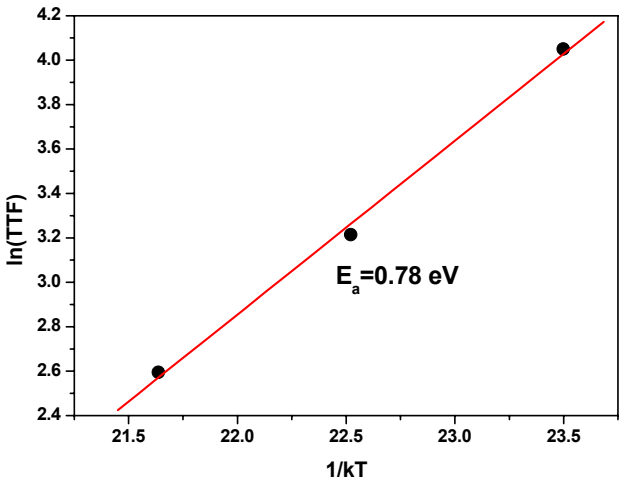

Figure 4.23. *The plot of lifetime as a function of reciprocal temperature for determining the activation energy Current density of 8mA/μm².*

Therefore, the result of the activation energy is not yet representative for the activation energy of the failure process. For an accurate measurement of the activation energy, a larger number of devices need to be tested, which was beyond this study.

4.5 Conclusions

An experimental study into electrothermomigration has been presented. A special test structure has been described, which allows temperature gradient to be locally imposed and measured along the length of the metal line. The experimental results have shown that the electromigration lifetimes in the presence of a temperature gradient are much shorter than those in a uniform temperature, in which the uniform temperature is kept at the same value as the peak temperature in the presence of a temperature gradient. Results also show that both electromigration tests in uniform temperature and the presence of a temperature gradient are proportional to j^{-n}. With a correction for the Joule heating, the MTF and j are well fitted to the Black equation, and an acceptable n value has been found of about 2.9 for uniform temperature test results. However, the fit is not good enough for the temperature gradient test results, and the observed n value of 4.3 is too high compared with literature. This clearly indicates the effect of a temperature gradient on the current exponent. This observation is extremely important when the test result is used to extrapolate the lifetime for use condition under temperature gradient environment. In power IC metallization where the hot spot from an

active device may be more than 10°C hotter than nearby regions, this suggests that the metallization examined under the presences of a temperature gradient would be very meaningful for electromigration design rule of power ICs. It is shown that a higher temperature gradient results in a stronger reduction of the electromigration lifetime, the temperature gradients in this experiments are similar with those in commercial power IC's. This is to point out a threat of EM failure in power IC's metallization this is a concern for overall reliability of power ICs to improve existing design rule.

A typical application of this technique has been demonstrated, in which a test module is designed and fabricated for measuring the activation energy using commercial test equipment. The acceleration of electromigration test can be done without increasing the current density and the ambient temperature up to high values.

The modelling of the failure mechanism has shown that the reduction of the electromigration lifetimes in the presence of a temperature gradient is determined by the effect of the temperature gradient on the electromigration-induced failure, rather than an additional driving force by thermomigration. This is in qualitative agreement with recent theoretical modelling [5]. This work demonstrates the importance of temperature gradients as a source of electromigration flux divergence in power IC metallization and therefore the necessity of controlling the temperature distribution in an active power IC in order to improve its lifetime.

4.6 References

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CHAPTER 5

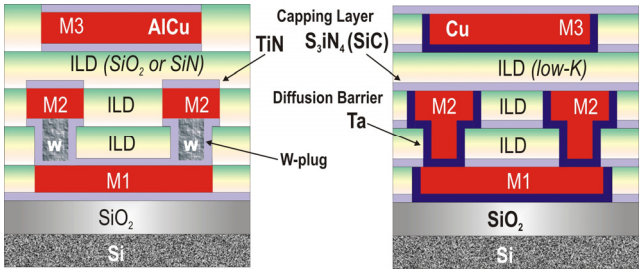
Effect of Interconnect Layout on Electromigration

CONTENTS

As the VLSI circuitry becomes denser, multilevel metallization interconnects has to be vertically stacked in a multi-level system (currently more than 7 levels) connected vertically by vias or plugs. Therefore, beyond the features that affect the multilevel interconnect reliability discussed in previous chapters, the electromigration via failure is a great threat not only because it ultimately destroys the device but also, perhaps more importantly, because it causes functional degradation. This chapter presents an investigation of effects of multilevel interconnect layouts on reliability improvement to electromigration through simulation and experiment. Different via and reservoir layouts that are encountered in several real-world designs are characterized by simulation and experiment. A 2D simulator is used to model the stress evolution and failure. An extensive experiment is done to compare with the simulation observations. The simulation and experimental results come to the same conclusion. This strongly confirms that the 2D simulator is a good tool to predict the electromigration reliability in the design phase in a quick and cheap way. The effect of current crowding due to interconnect layouts on the electromigration will be also discussed.

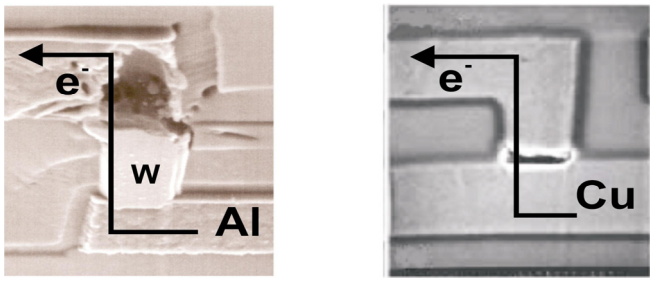
5.1 Introduction

Electromigration failure of a via/contact in multilevel interconnects used in integrated circuits (ICs) occurs by the formation of voids in the metal line. As device features reduce in ultra-large-scale integrated circuits (ULSI), the amount of metal that needs to be removed due to electromigration from the via/contact area to cause a failure decreases. Therefore, electromigration is becoming an increasingly important aspect in IC-reliability. In light of this, the interconnect layout features are becoming more and more important for the electromigration reliability. It has been recognized that the electromigration behaviour in W-plug/metal stripe structures is different from conventional metal-strip structures because there is a "blocking boundary" for AlCu, which is formed by a W-plug connecting two metal layers. The electromigration failures occur much more readily in or near the area of the W-plug than in the metal-strip structures because metal atoms are forced away from the via/contact by an electrical current, while the metal ions cannot flow through the blocking boundary to fill the vacancies around the via/contact area.



(a) ***(b)***

Figure 5.1. *A cross-section of typical multilevel interconnects;* ***(a)*** *Al-Si-Cu metallization,* ***(b)*** *Cu metallization.*



(a) ***(b)***

Figure 5.2. *The typical failure open circuit in Al metallization, (a) and Cu metallization (b).*

Consequently, the void formation at a W-plug can cause an open circuit. Unfortunately, this typical failure mechanism of Al interconnects as shown in Figure 5.2.a is also observed in modern Cu interconnects due to electromigration [1] as well as stress-voiding [2] as shown in Figure 5.2b. Therefore, this issue is still of prime importance to future interconnect developments. It is well known that the electromigration lifetime of multiple-level interconnects is influenced by the presence of a "reservoir" around the via/contact. Reservoirs are defined as metal parts that are not or hardly conducting current that act as a source to provide atoms for the area around the blocking boundary where the atoms migrate away due to the electrical current. The lifetime of interconnect systems can be prolonged by using the reservoirs, which is called "reservoir effect". Several authors have experimentally shown the reservoir effect [3-8,13]. The reservoir can be created by an increase of the overlap, the number of vias/contacts and the use of end-cap upstream from the electron flow. The experimental data from literature clearly show that the lifetime increases with an increase in reservoir area as well as with an increase in the number of vias/contacts. Most authors have reported that the structures with multiple-via/contact always have a larger reservoir area compared to structures with single via/contact. However, whether the lifetime prolongs due to increasing the number of vias or the reservoir area is not clear yet. Furthermore, whether the reservoir and vias layouts in vertical (perpendicular with current stress) or horizontal (parallel with current stress) direction will be better for electromigration reliability improvement is still a question. This is very important in case the space is limited in one direction of the chip. These imply that there is still a great demand for better understanding of the electromigration-induced failure mechanism of multilevel interconnects to improve the electromigration by introducing new design-schemes.

The aim of the work described in this chapter is to characterize an effect of multilevel interconnect layout on electromigration performance through simulation and experiment. The simulation results are compared with experimental data from us as well as literature with the aim to demonstrate the usefulness of a 2D simulator in predicting electromigration performance of interconnect layouts in a cheap and quick way during the design phase. In following section, a study dealing with computer simulation using an electromigration simulator will be presented. Thereafter, an extensive

experiment and simulation for comparisons will be shown. Then, the effect of current crowding on electromigration performance in the reservoir, which is observed through experiment, is discussed to extend the model which is currently used in the electromigration simulator. Finally, a possible use of the 2D simulator to predict possible failure locations is demonstrated, and the results are also compared with the observation from failure analysis.

5.2 Electromigration simulation for the layout effect

In this section, first, physical electromigration model implemented in the 2D simulator is briefly described. Then the simulator is used to characterize the effects of the reservoir area, reservoir layout, multiple-via, via layout, and current sharing on electromigration lifetime. The tensile stress build-up at the cathode is considered as an important parameter for the failure evolution because it can cause void open circuit when a critical stress is reached. Therefore, the critical stress is used to estimate the electromigration lifetime in this investigation.

5.2.1 Electromigration model description

The atomic flow due to electromigration is modeled using a vacancy mechanism. In the model both electromigration and stress migration are described in terms of the evolution of vacancy concentration. Basically, the model is based on the Clement's and Thompson's model [3], using Hooke's law for elastic deformation. The continuity equation for vacancies can be written as follows;

$$\frac{\partial C_V}{\partial t} + \Delta J_V = -\frac{1}{B\Omega}\frac{\partial \sigma}{\partial t} \tag{5.1}$$

Where C_V is the vacancy concentration, B is the bulk modulus, Ω is the atomic volume, and J_V is the flux of vacancies. The right part of equation 5.1 is the sink/source obtained by using Hooke's law. J_V is composed of a drift and a diffusion current, expressed as follows:

$$J_V = -D_V \nabla C_V + \frac{D_V C_V}{k_B T} Z^* eE \tag{5.2}$$

Where D_V is the vacancy diffusivity, $k_B T$ is the thermal energy, Z^* is the effective charge number, e is the elementary charge, and E is the electric field.

The resistivity of a metal line is related to the stress evolution according to the piezoresistive effect [4].

$$\frac{1}{\rho}\frac{\partial \rho}{\partial \sigma} = K_P \tag{5.3}$$

Where ρ is the resistivity, $K_p=1.2\times10^{-5}$ MPa^{-1} is the piezoresistive coefficient for aluminium. The vacancy concentration C_v in the presence of a hydrostatic stress σ is

$$C_V = C_o \exp\left(\frac{\sigma\Omega}{kT}\right) \tag{5.4}$$

Where C_0 is the vacancy concentration in the absence of any stress effects. From equation (5.3) and (5.4) the relation of vacancy concentration and resistivity can be written:

$$\rho = \rho_o\left(\frac{C_V}{C_o}\right)^{\gamma} \tag{5.5}$$

Where ρ_0 is the initial resistivity, and $\gamma = kTK_p/\Omega$.

This is just a brief description of the system of equations that have been used in the simulator, more detail can be found elsewhere [5].

5.2.2 Simulation structures and conditions

The simulation structures were designed varying the overlap, the reservoir area, the reservoir layout directions (vertical and horizontal), the number of vias and the via placement directions. The structures as shown in Figure 5.3 (a), (b), and (c) have the same left and right overlap but different end overlap (different reservoir area); Figure 5.3 (c) and (d) have the same reservoir area but difference in layout direction; Figure 5.3 (a), (e) and (f) have the same overlap but difference in number of vias; Figure 5.3 (c), (d), (e) and (f) have the same reservoir area but difference in number of vias; (e) and (f) have the same reservoir area and number of vias but differ in vias placement. In each structure, the width and length (from the edge of cathode to the edge of anode) of the metal lines were kept as 3μm and 72μm respectively. The size of contact/via is $1\times1\mu m^2$. In Figure 5.3 only a part of the metal line is shown. The reservoir area is in this paper defined as the amount of aluminium surrounding the via or upstream from the electron wind (including the via/contact).

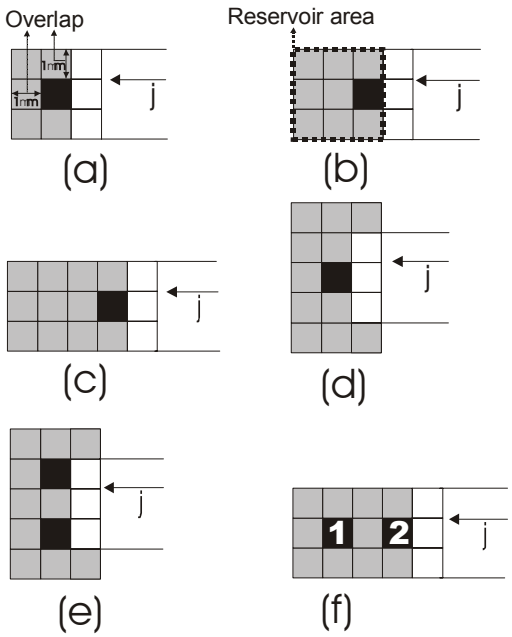


Figure 5.3. *Simulation structures for the single and two vias/contacts configurations with varying reservoir area and overlap. The reservoir is located upstream with respect to the electron flow.*

The metallization lines have been stressed in the simulator with a current density of $J=10mA/\mu m^2$, at temperature $T=200^oC$. During the electromigration stress, the current is forced from the anode side flowing through contacts at cathode (grounded zero resistance) out the line. In this study, we only focus on the stress build-up (tensile stress) at the cathode end, where the voids will be formed that ultimately lead to open circuits.

5.2.3 Simulation results and discussion

Reservoir effect

As mentioned above, in these simulations, tensile stress at the cathode side is used for analysis of the electromigration behavior in this study. The failure times are taken when the tensile stress reaches a critical stress (the stress that a metal line can sustain before the open circuit). Figure 5.4 shows the stress distribution at the cathode side of structures (a) and (f) in Figure 5.3 as an example. It is observed that the right edge of the contact always sustains a highest tensile stress. From now on, the maximum tensile stress at the right edge of the contacts is used to analyze the electromigration lifetime.

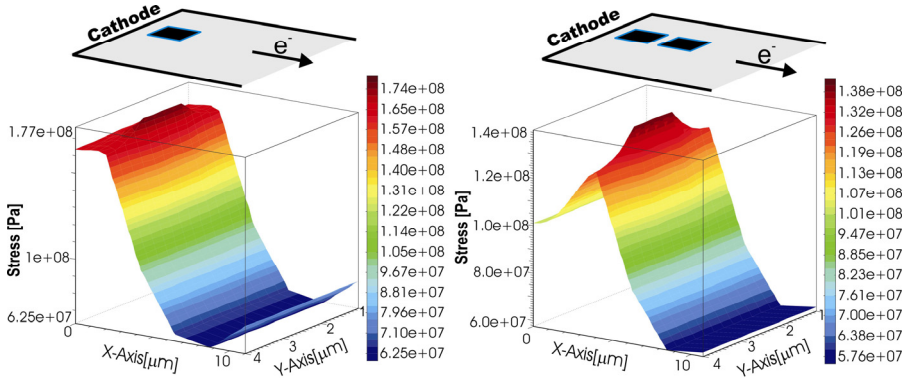


Figure 5.4. *Stress distribution at cathode site after 400 hours of current stress: (a) of structure 5.3a; (b) structure 5.3f (see Figure 5.3).*

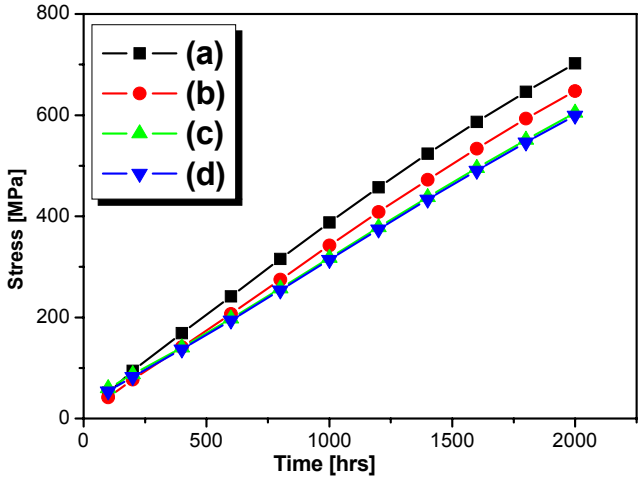


Figure 5.5. *Evolution in time of the maximum stress taken at the right edge of the via, (a),(b),(c),and (d) denote the different reservoir configurations as shown in Figure 5.3.*

To illustrate the reservoir effect, the simulation results of the layout with different reservoir areas as shown in Figure 5.3 (a), (b), (c) and (d) were selected for comparison. Their tensile stress evolution as a function of time is shown in Figure 5.5. It can be seen that an increase in the reservoir area (serve as sacrificial metallization) leads to a decrease in stress build-up. Increasing the reservoir area in the horizontal or vertical direction (compare Figure 5.3 (c) and (d)) gives no difference in the stress build-up at the cathode via. This indicates that the reservoir area plays a more important role than the reservoir layout in delaying the evolution of tensile stress. Previously reported experimental data [7,8,10] have the same observation. Published data in [8,10]

showed the lifetime prolongation due to the increase the length of reservoirs (or reservoir area). The work from Atakov [7] showed that the reservoirs in various directions give almost the same lifetime, confirming our comparison of structures (c) and (d).

Multiple-via/contacts effect

Figure 5.6 shows the maximum tensile stress build-up at the right edge of the via (via number 2 in case of Figure 5.3 (f)) obtained from simulation structures (a), (e) and (f) in Figure 5.3. It is clearly shown that the stress build-up in time of the structure with single via is higher than that of the structure with two vias. That means the lifetime of the structures with two vias is longer comparing to the structures with single via, because the time to achieve a critical stress due to electromigration, which can cause an open circuit is longer. This can be explained by the fact that the structures with two vias have a larger reservoir area compared to the structure with single via. Experimental data from the literature [7,9] showed comparable results. However, the question needs to be answered whether the lifetime is increased due to the increase in the reservoir area or the increase of the number of vias. To verify this situation, we have selected the simulation results of structures as shown in Figure 5.3 (c), (d), (e) and (f), in which the reservoir area is kept the same and there is one more contact in reservoir areas in vertical or horizontal direction.

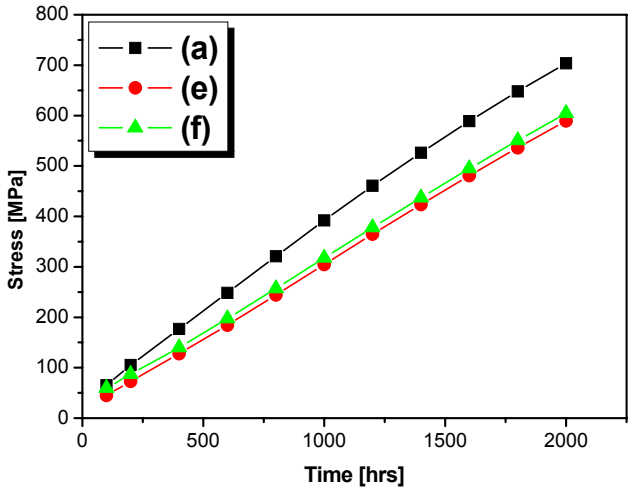


Figure 5.6. *Stress builds up taken at the right edge of the contact for constant overlap configurations seen in Figures 5.3 (a), (e) and (f).*

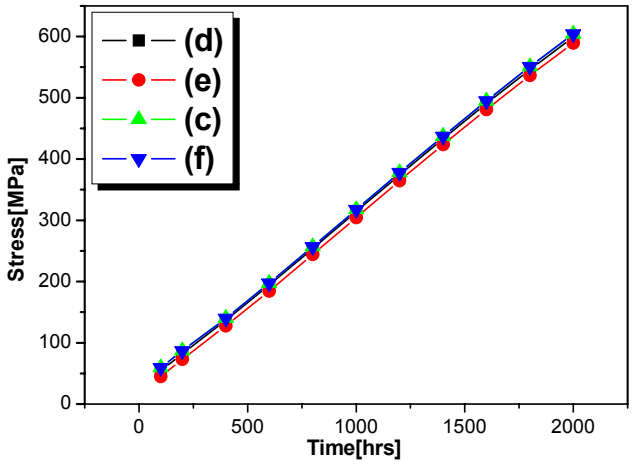


Figure 5.7. *Stress build-up at the right edge of the vias (number 2) for a constant reservoir area with the via configurations of (d), (c), (e), and (f) in Figure 5.3.*

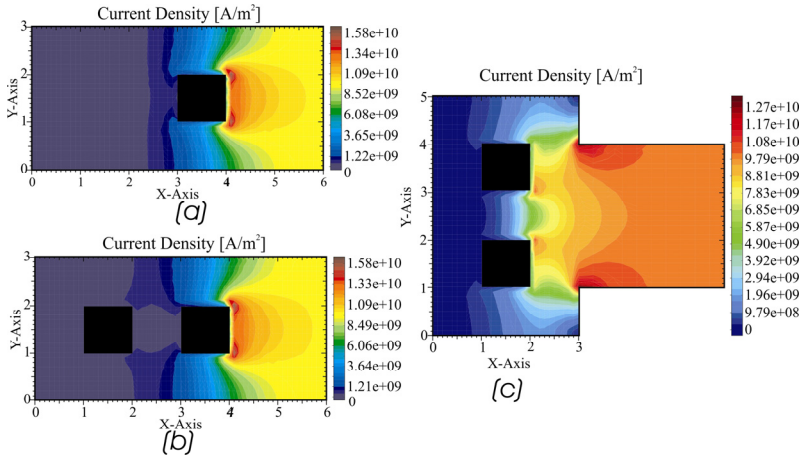


Figure 5.8. *The current distribution of structures with 1and 2 via (horizontal and vertical) layouts.*

Their maximum stress build-up at the right edge of via (the via number 2 in case of two vias in horizontal) is shown in Figure 5.7. It can be seen that there is no difference in stress build-up for these structures. In other words, the multiple-via and single via structures have the same the electromigration lifetime as long as the total reservoir area is the same. However, the multiple-via layout would reduce the early failures due to the misalignment during technology process [11]. This also means that the effect of current sharing in the multiple-via is significantly less important than the total reservoir area because the electron flow direction is different in these structures.

To explain these situations, we look at the current distributions in these cases. The simulation results of current distribution for the cases of single and two vias in horizontal and vertical direction as illustrated in Figure 5.8 show that they are very similar at the right-most edge of the via nearest to the line (via number 2 in case of structure (f) in Figure 5.3). This means that in the structure (f) almost all current flows through the via number 2. Comparing the current distributions in the cases of two vias in horizontal and vertical configuration as shown in Figure 5.8, we found that there is only minimal reduction in current distribution at the vias in structures with the vertical vias. This is due to the current sharing effect in this structure, and maybe current crowding plays a role as well, which will be discussed in the next section together with the experimental results. The result is that the stress build-up in time is slightly smaller in the structure with 2 vias in vertical direction compared to that in horizontal direction. These simulation results are comparable with the experimental data from Dion [17]. This author also reported that adding more vias in the same reservoir area has negligible impact on the lifetime. In cases of two vias in vertical and horizontal directions with the same reservoir area, the experimental data from Atakov [7] show that they have the same electromigration lifetime.

Current sharing effect

It can be recognized that the effectiveness of the current sharing effect depends on the schematic layout. When current sharing takes place, a multiple-via layout would prolong the electromigration lifetime of multilevel metallization as reported in the literature [9,12]. The experimental data from Le et al. [9] reported that the increase of the number of vias could result in a significant increase of the electromigration lifetime, or not, depending on the schematic layout. In our point of view, depending on the schematic layouts, there are two cases of current sharing in multiple-via as demonstrated in Figure 5.9. The first case shown in Figure 5.9(a1) and (a2) is to demonstrate that there is no current sharing in structure with 2 vias. This means that almost all current goes through only one via, this was reported by Ting [14] and Kawasaki [18]. In this case, adding more vias in the same reservoir area will not result in an enhancement of the electromigration lifetime. The unstressed vias area serves as a source of Cu and Al atoms to replenish the via area prone to electromigration failure.

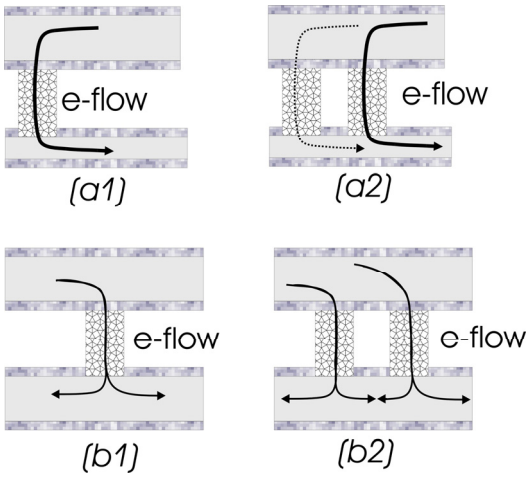


Figure 5.9. *The current density sharing effects in different schematic layouts.*

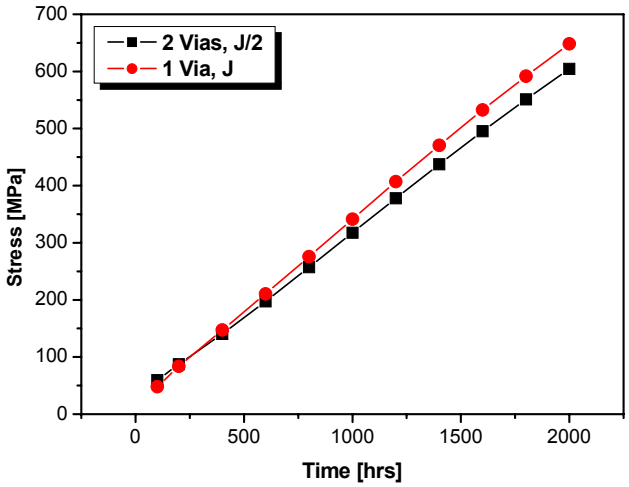


Figure 5.10. *The stress build-up in case of current density of J for single via and J/2 for two contacts at each via as shown Figure 5.3 (c) and (f).*

This situation was shown in the previous section. In the second case, as shown in Figure 5.9(b1) and (b2), described there is a current sharing between the vias. This indicates that the structures with multiple vias will carry a lower current density comparing to one with single via. The result is that the electromigration lifetime of multiple vias is much greater than single via as reported by Dion [12] and Le [9]. This situation is simulated by adjusting the current density going through each via (at the cathode side) of structure (f) (see Figure 5.3) to be J/2 (J is the current density in the metal line). The results are shown in Figure 5.10.

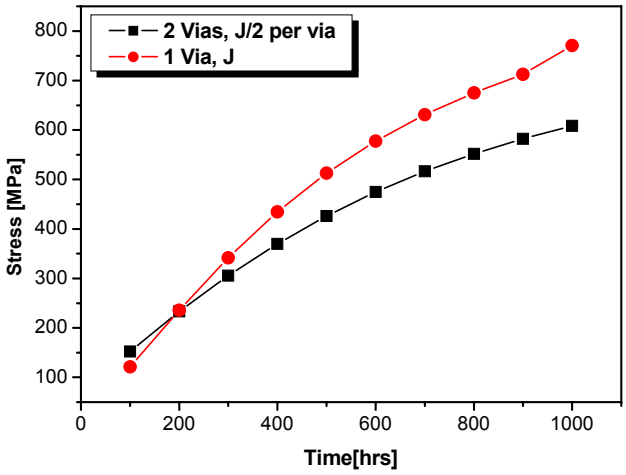


Figure 5.11. *The stress build-up in case of current density of J for single via and J/2 for two via layout and they have the same reservoir area. The layouts are similar with Figure 5.3(c) and (f), but the overlaps are much smaller.*

In this situation, we found that the right edge of the via number 1 sustains the highest stress instead of the right edge of the via number 2 as mentioned above. Although a current density of J/2 was forced through the contacts, the stress build-up is not much different comparing to single contact. It is our hypothesis that the effect of the reservoir area is more important than the effect of the current sharing because the vias are much smaller than the reservoir area. This hypothesis can be checked by carrying other simulations with structures similar (c) and (f) as shown in Figure 5.3, but these structures have larger via and smaller overlap compared with the structures (c) and (f). The via size is 3.2x3.2μm^2, the overlap and the end-cap is 0.4μm and the line width is 3.2μm. It is obvious that now the via is only slightly smaller than the reservoir area. The maximum stress build-up at the right edge of the via (via number 1 in case of two vias) reservoir area is shown in Figure 5.11. It has been found that the stress build-up is much larger in single via layout than in two via layout. That means the lifetime is much longer when the multiple vias is used, which proves the hypothesis that the relative size of reservoir with respect to via size can also play an important role respect to current sharing effect.

5.3 Electromigration experiment on the layout effect

In this section, the effects of the reservoir and via layout on the multilevel interconnect electromigration performance are extensively characterized

through a series of experiments. The results will be compared with the simulations to validate the simulation results, in which the simulation structures are designed to be more realistic and comparable with the test structures.

5.3.1 Test structures

The test structures are designed with variations in the reservoir area, the reservoir layout (vertical and horizontal), the number of vias and the via layouts. The structures with number of vias, N equals to (1x1), (1x2), (1x3), (1x4) are named row layouts, and the other structures with number of via, N equal to (2x1), (2x1+1), (2x2) are named square layouts as shown in Figure 5.12. The via size is (0.4x0.4)μm^2, line width and spaces between vias are 0.4μm. The line length and overlap are 100μm and 0.05μm in case of single via, and 800μm and 0.08μm in case of multiple-via, respectively.

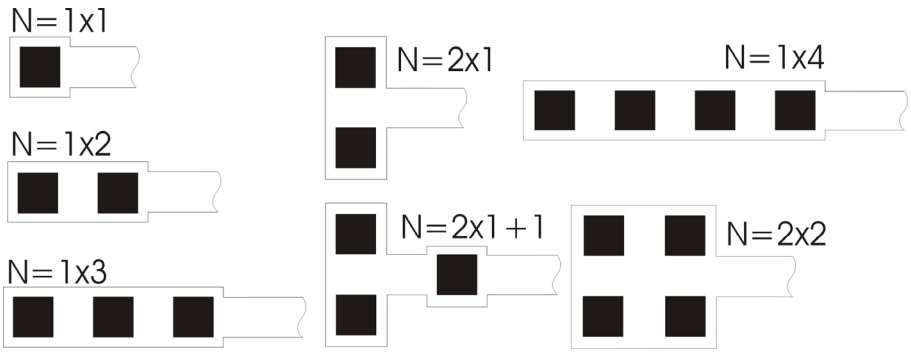


Figure 5.12. *The different reservoir and via layouts for experiments.*

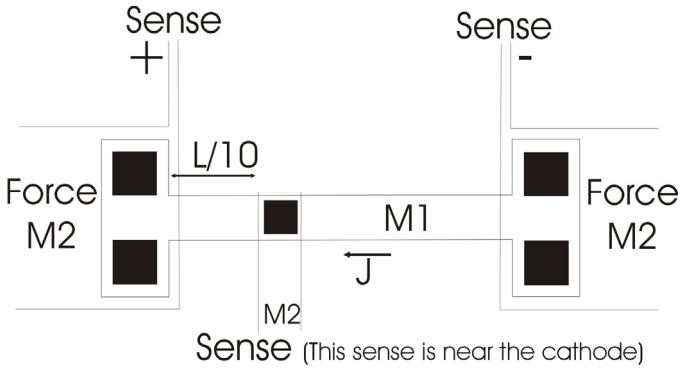


Figure 5.13. *Total layout of test structure.*

The test structures contain a sense lead near the cathode to measure the resistance change of the reservoir area during the electromigration testing (see Figure 5.13 for more details). These test structures were processed and encapsulated in ceramic package at Infineon Technologies AG. The packaged test structures were stressed in an oven at the temperature T=225°C, and the current density J=12.05mA/μm^2, except where mentioned otherwise.

5.3.2 Test results and discussion

The results of failure time distributions were statistically analyzed assuming a lognormal distribution following JEDEC standards [19]. The failure criterion is set to an increase of relative resistance change of 20%. The median time to failure (MTF) is extracted from the lognormal plot, in which the inverse cumulative distribution function (INV_CDF) is plotted as an exponential function of failure times. Figure 5.14 shows failure distributions for structures with 1 via, (1x1) and 2 vias in row, (1x2) and square, (2x1). The distributions are well behaved with generally similar slopes. It can be seen that the MTF of the 2 vias structure is more than two times higher compared to 1 vias. The MTFs of row and square are not much different. The electromigration results observed from structures with 3 vias layout in row (1x3) and square (2x1+1) shows the same conclusion (see Figure 5.15). Even though, the configuration of 2 and 3 vias square layouts is quite different.

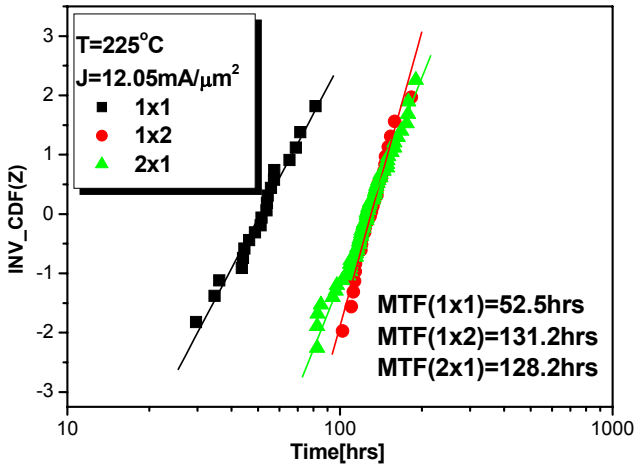


Figure 5.14. *Failure time distribution for single via and two vias (row and square see Figure 5.12).*

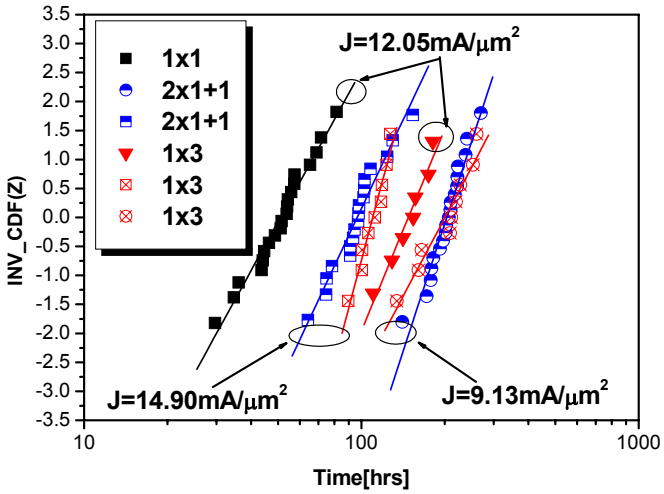


Figure 5.15. *Failure time distribution for 1 via and 3 vias (row and square see Figure 5.12), various current densities.*

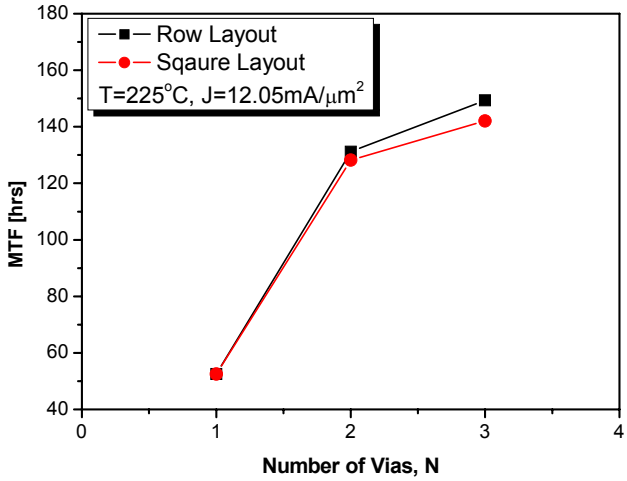


Figure 5.16. *MTF as a function of the number of vias for row and square layouts.*

It should be mentioned that the test result of structure 3 vias in square (2x1+1) at current stress of 12.05mA/μm^2 is missing. Therefore the MTFs of structure (2x1+1) at stress current of 9.13mA/μm^2 and 14.9mA/μm^2 are used to extrapolate the MTF at current stress of 12.05mA/μm^2. These results indicate that the failure time distributions for multiple-via is determined by the number of vias, rather than the via layout. This also shows that the effects of current sharing are less important than the reservoir area.

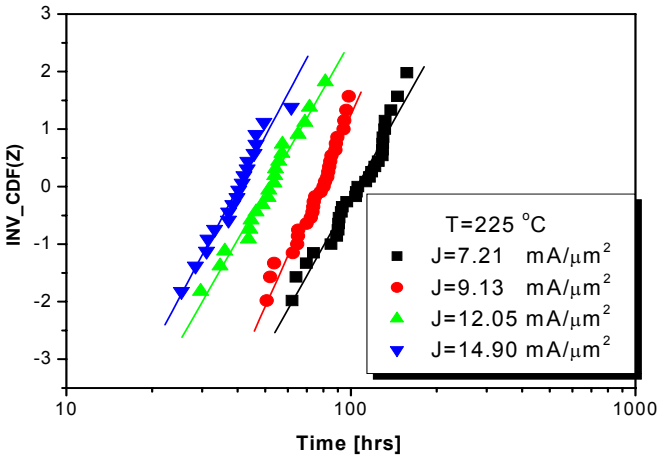


Figure 5.17. *Failure time distribution for a single via with testing of different current densities.*

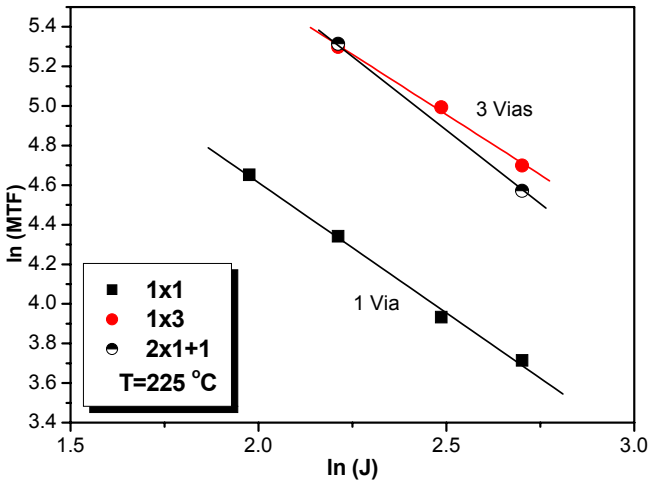


Figure 5.18. *MTF as a function of current density, for 1 vias and 3 vias layouts, see Figure 5.12.*

These experimental observations confirm qualitatively the simulation of stress build-up. Figure 5.16 shows that the MTF is a nonlinear function of the number of vias, and it seems to saturate when the number of vias continues to increase. The increase in the number of vias is associated with the increase of reservoir length. Le et al. have recently reported that when the reservoir length increases to a critical value, there will be no more increase of the lifetime when the reservoir length increases further [20]. The electromigration tests were carried out with different current densities for 3 vias and 1 via to

verify the current density dependence. The failure time distributions are shown in Figure 5.15 and Figure 5.17 for 3 vias and 1 via, respectively. The MTF as a function of current densities for 3 vias and 1 via is shown in Figure 5.18. It can be seen that there is very similar current density dependence for these cases.

5.3.3 A comparison with simulation

To compare between experiments and simulations, the tested and simulated structures are designed with the same geometries. The dimensions of simulation structures are as follows: via size is (3.2 x 3.2)μm^2; the space between two vias is 3.2μm (on horizontal as well as vertical direction); and the overlap is 0.4μm. Line length (does not include the reservoir length) and width of all simulation structures are kept the same at 45.2μm and 3.2μm respectively. The resistance change in the reservoir area is an important aspect in this study so simulation mesh in the reservoir area is meshed much finer than in the other areas of the simulation structures. The total relative resistance change in the reservoir is calculated from the obtained resistance distribution using a so-called P-S model. In the P-S model, the resistance along each row (parallel to the length) is first calculated, and the total resistance is the obtained by treating the rows as being connected in parallel. The equation for relative resistance change calculation using the PS model is as follows:

$$\frac{\Delta R_T(t)}{R_T(0)} = \frac{n_w}{n_l}\sum_{i=1}^{n_l}\left\{\sum_{j=1}^{n_w}\left[1+\left(\frac{\Delta R(t)}{R(0)}\right)_{ij}\right]^{-1}\right\}^{-1} - 1 \qquad (5.7)$$

Where $\Delta R_T(t)/R_T(0)$ is the total relative resistance change at time, t , n_l and n_w denote the number of node along the length and across the width, respectively. $(\Delta R(t)/R(0))_{ij}$ is relative resistance change at the i^{th} and j^{th} node. All simulations were done at a current density J=12.05mA/μm^2 and temperature T=225°C, except when mentioned otherwise. A failure criterion of 5% resistance increase is used. The 20% would be unrealistic and too time consuming. However, the use of the smaller failure criterion will not influence the comparison of simulations and experiments, because the comparisons are made after making the normalization as will be discussed detail as below. Figure 5.19 shows the simulation results of resistance change for 1, 2, and 3

vias. It can be seen that the resistance increase of the single via layout is faster than the multiple-via layout. This means that the electromigration lifetime is shorter for the single via layout. The resistance change of multiple-via in row and square layout are almost the same. The structures with 3 vias in row and square layout have a small difference in resistance change due to a small difference in reservoir area between the two layouts. This difference cannot be overcome due to restrictions in the design of the simulated structure. MTFs were estimated and shown in Table 5.1.

Table 5.1. *The results of MTF in cases of simulations and experiments*

Structure Name	J [mA/μm^2]	**MTF** [hrs] (Experiment)	**MTF** [hrs] (Simulation)	**T [°C]**
1	12.05	53	240	
1x2	12.05	131	455	
2x1	12.05	128	441	
1x3	12.05	149	735	**225**
2x1+1	12.05	142*****	727	
1x3	14.90	204		
1x3	9.13	111		
2x1+1	14.90	99		
2x1+1	9.13	205		

** This value is extrapolated from the other electromigration experiments*

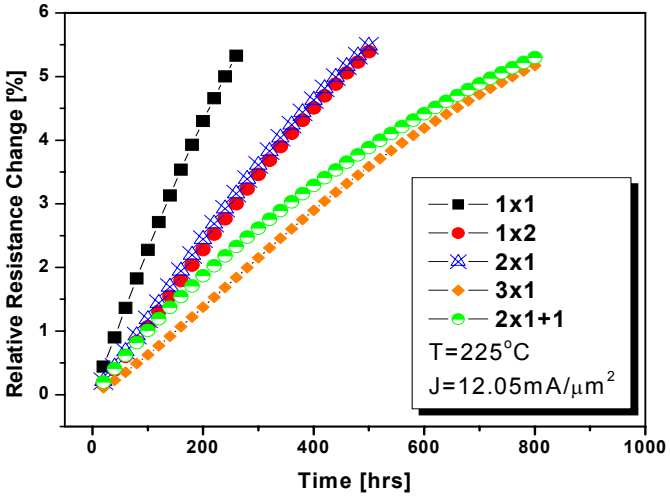


Figure 5.19. *Simulation of relative resistance change versus time of single and multiple-via structures.*

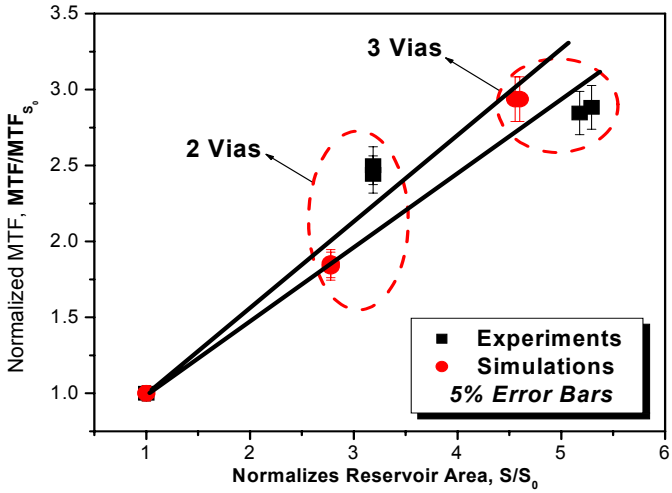


Figure 5.20.*Normalized MTF versus reservoir area for J=12.05 mA/μm².*

To compare between simulation and experiment quantitatively, we plotted the normalized $MTF_{multiple\text{-}via}/MTF_{single\text{-}via}$ against the normalized area, $Sr_{multiple\text{-}via}/Sr_{single\text{-}via}$ with error bars of 5% as shown in Figure 5.20. This error is acceptable and this simulation can be useful for a quick and cheap electromigration reliability prediction.

5.4 Current crowding effect in multiple-via layout

The current crowding effect, which is considered as driving force to assist the electromigration process, will be discussed through the simulation and experimental observations in this section. This effect is in debate between several authors [21-23]. With the continuous scaling of the feature sizes of ICs, current crowding can be an important concern. Tu et al. have recently reported the effect of current crowding on the electromigration performance of multilevel interconnects [21]. Hence current crowding is considered as a driving force that can assist the electromigration process. In this section, this effect will be characterized through experiment and simulation. The simulations were carried out with a different current stress for structures for 2 vias layouts (row and square). When the current density increased from 12.05mA/μm^2 to 19.66mA/μm^2 (increase of 63%), the difference in electromigration lifetime between row and square layouts was still small (see Figure 5.21). The electromigration tests were carried out with structures of 4 vias in square and row layouts (see Figure 5.3 with the structures, N=1x4, and N=2x2).

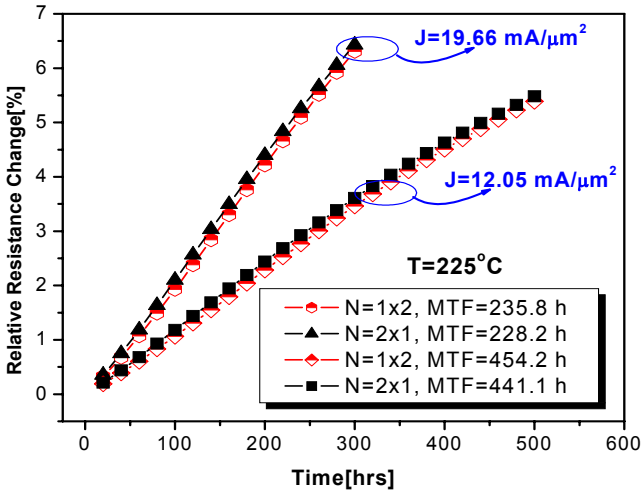


Figure 5.21. *Relative resistance change versus time simulations for 2 vias layouts (row and square) at different stress current.*

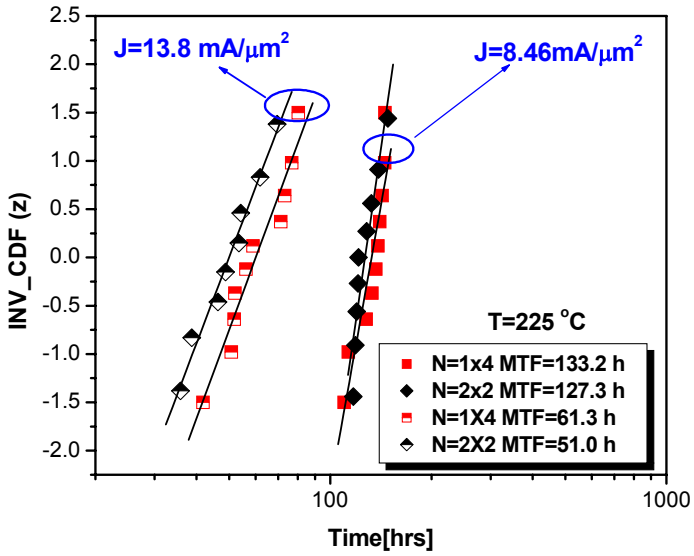


Figure 5.22. *Failure time distribution of structures with 4 vias (in row and square).*

It should be mentioned that these test structures were processed in a different technology from the test structures with 1, 2, and 3 via in pervious sections. The test structures were stressed at temperature T=225°C and current densities J= 8.46 and 13.80mA/μm^2. The lognormal failure time distributions for these cases are shown in Figure 5.22. The experiments show that when the stressing current is increased from 8.46 to 13.8mA/μm^2 (an increase of

63% like in the simulation), there is a slight increase in the difference of electromigration lifetime between row and square layouts. This means that the current crowding affects the electromigration lifetime but it is a very small effect. The simulation results did not show this effect because it was not incorporated in the simulator yet. The simulation of electromigration is based on a well-known equation for vacancy flux that composes of drift and diffusion current as demonstrated in section 5.2:

$$J_v = -D_v \nabla C_v + \frac{D_v C_v}{kT} Z^* eE \tag{5.8}$$

Where C_v is the vacancy concentration, D_v/kT is mobility, and D_v is the diffusivity of vacancies in the crystal. Recently, Tu et al. have proposed another mechanism of vacancy diffusion due to the current crowding. A driving force due to current crowding can enable the vacancies diffuse from the high to the low current density regions [21]. This means that there is an additional driving force to assist the vacancies from the reservoir area (low current density) to the high current density areas (at current crowding regions). In this situation, when vacancy flux approaches the cathode, vacancy diffusion by the current gradient (due the current crowding) from the high to the low current density regions need to be included in the total vacancy flux as follows:

$$J_v^{Total} = -D_v \nabla C_v + \frac{D_v C_v}{kT} Z^* eE + \Delta C_v \left(\frac{D_v}{kT}\right)\left(\frac{dP}{dr}\right) \tag{5.9}$$

Where ΔC_v is the excess vacancy concentration in high current crowding region relative to the constant flux region, (dP/dr) is the driving force due to current density gradient as in current crowding. P is the potential energy for an excess vacancy driven by the current density *j*, and it is calculated as follows;

$$P = q_v |j| A \Delta \rho_v \tag{5.10}$$

Where q_v is the charge of vacancy, A is the scattering cross section of the vacancy, and $\Delta\rho_v$ is a resistance due to an excess vacancy in the Al crystal. A more detailed calculation of this driving force is given in [21]. Therefore, the current crowding effect should be taken into account for a better simulation. As can be seen in equation (5.9), the current crowding adversely affect the electromigration lifetime. When the current density in the metal line is not

high enough or dimensions are large enough, the effect of current crowding can be ignored, as experimentally reported by Atakov et al. [7] and our experimental data so far. It is recognized that this effect will be very important when the metal line is shrunk because the current gradient due to current crowding increases very much when the dimensions decrease. Apparently, when the current density is kept unchanged and dimensions reduce, the driving force of electron wind (F_{wd}) for electromigration remains unchanged, while the driving force (F_{grad}) by current gradient (due to the current crowding) increases. Yeh and Tu [24] have reported that for the line width of 1μm, the driving force ratio F_{grad}/F_{wd} can be about 0.2, and when the line width is 0.25μm, the F_{grad} becomes even larger than F_{wd}.

To clearly demonstrate the effect of current crowding on the electromigration lifetime, we have carried out another set of electromigration experiments (new design and process of test structures, and new test condition). Special test structures are designed to create large differences in the current crowding as shown in Figure 5.23. The structures in Figure 5.23(a) and (b) are designed with a reservoir layout large enough for 2 contacts, but only one contact is used. The reservoir areas are the same for the two structures. The structures in Figure 5.23(c), (d), and (e) are designed with reservoir layouts large enough for 4 contacts, but only 2 contacts are made, and the reservoir areas are the same for the three structures. The dimension of the contacts are $(0.4x0.4)\mu m^2$. The width is 0.4μm, and the overlay is 0.08μm. The forces and senses for electromigration test are laid out the same as in Figure 5.13. The electromigration tests are done at a current density of $15.92mA/\mu m^2$ and a line temperature of 250°C. The electromigration results on the structures with a single contact are shown in Figure 5.24.

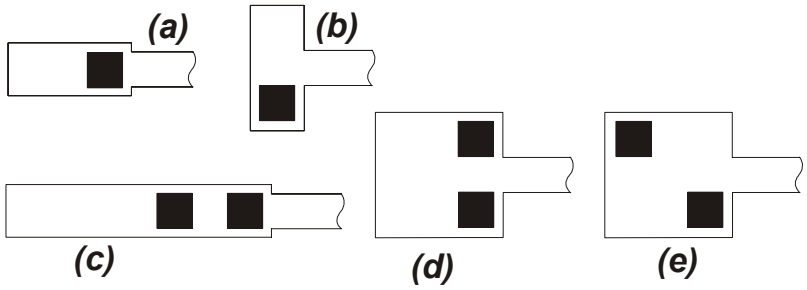


Figure 5.23. *Test structures to study a current crowding effect on electromigration lifetime.*

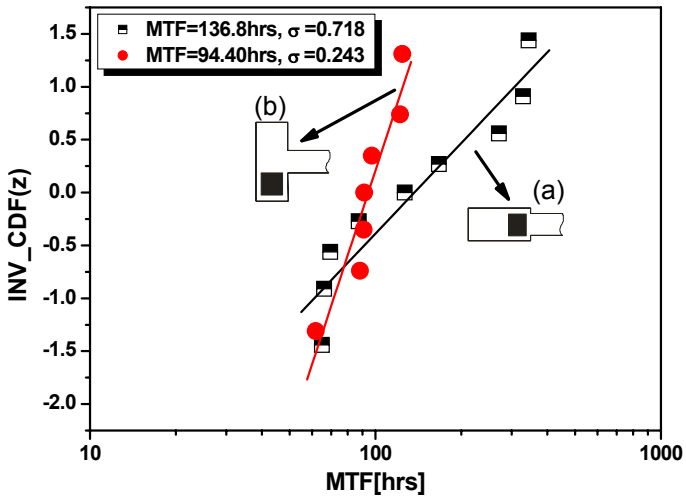


Figure 5.24. *Failure time distribution of structures Figure 5.23(a) and (b).*

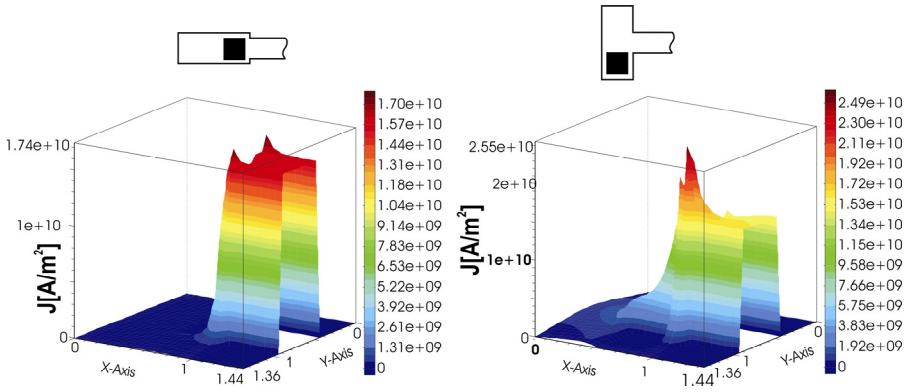


Figure 5.25. *The current distributions of structures Figure 5.23(a) and (b).*

It can be seen that the electromigration lifetime of structure (a) (see Figure 5.23a) is larger than that of structure (b). This is due to the reduced current crowding in structure (a) compared to that in structure (b). As can be seen from Figure 5.23 that in structure (b), the current from the metal line is detoured at a 90° corner before entering the contact, and this does not happen to structure (a). The current distributions are simulated for the two structures as shown in Figure 5.25. The current gradient due to the current crowding around the contact in case of structure (a) is lower than that in structure (b). The higher current gradient around the contact in structure (b) can build up a higher extra electromigration driving force that can result in the shorted electromigration lifetime compared to the case of structure (a).

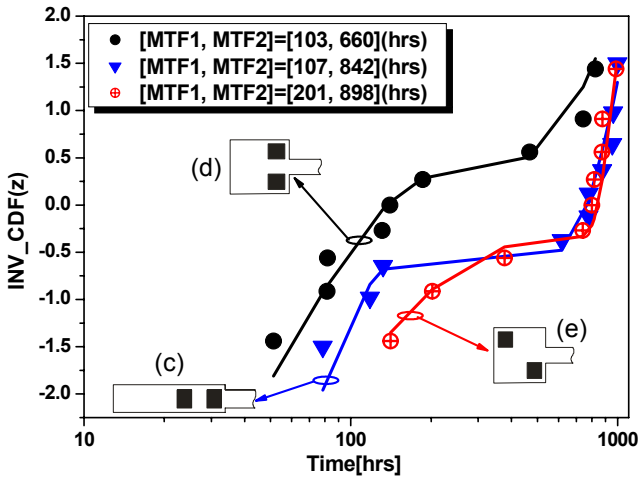


Figure 5.26.*Failure time distribution of structures Figure 5.23(c), (d) and (e).*

An estimation from the simulation results shows that the ratio of the peak current in structure (b) and (a) J^{b}_{peak} /J^{a}_{peak} is about 1.5. It is observed that the median reduction of the electromigration lifetime due to the current crowding is about 30%. Therefore, a high current crowding (due to high current density and the layout) plays an important role in electromigration reliability.

In the multiple-via layout, the current crowding effect on the electromigration lifetime is also observed. As can be seen on Figure 5.26, the results of electromigration tests on structures (c), (d), and (e) (see Figure 5.23) clearly depicts that the electromigration lifetime of structure (d) is shorter compared to structures (c) and (e). Apparently, in structure (d), the current is detoured at both contacts, and the current crowding occurs at both contacts. This can imply that the failure evalution at both contacts is properly taking place at the same time, resulting a short electromigration lifetime compared to structures (c) and (d). As can be seen in Figure 5.26, the failure time distributions seem to follow a bimodal distribution. A high rate of early failures is observed in case of structure (d). It can be seen that for contact layouts like structures (c) and (f), the current crowding may occur at one contact. Less current crowding on the second contact (the contact on left-behind) can be a fact that results in a less early failure with structures (c) and (f).

5.5 Predicting possible failure locations

The simulator can be used to calculate the stress build-up distribution. Therefore, it can be used to predict the voiding location due to

electromigration because the void and the tensile stress are associated. In Figure 5.27, the distributions of tensile stress in the reservoir area are shown to be associated with voiding from failure analysis by SEM for cases with single via and 3 vias in a row. We observed that the voids appear at a location where we found the maximum tensile stress build-up in simulation. In case of multiple-via structures, the void preferably occurs at the vias closest to the line as can be seen from SEM image of three via structures. Similarly, the simulation result of tensile stress distribution shows that the stress at via closest to line is highest compared to the other locations. This is due to the fact that the current sharing did not occur in the three via structure for both simulation and experimental situations. The good agreement between simulation and failure analysis observations point out that the simulator tool can be used to predict the failure location during the design phase, and the electromigration reliability can be improved accordingly.

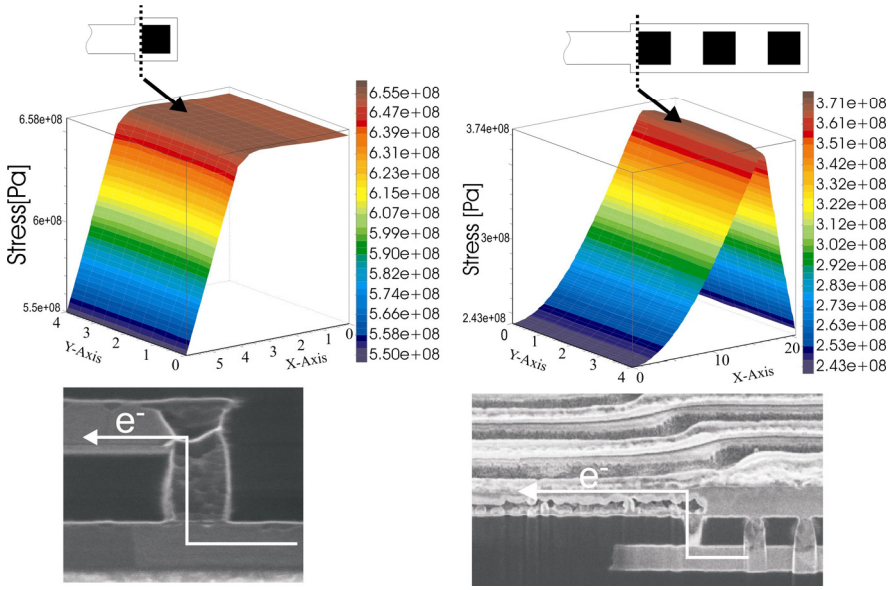


Figure 5.27. *Stress build-up distribution from simulation and voiding observations.*

5.6 Conclusions

Characterizations of the reservoir and via layout have been carried out through simulations and experiments and their results are found to be comparable. Both experiment and simulation have shown that by increasing

the number of vias and the reservoir area, the electromigration lifetime is increased. If two layouts have the same reservoir area, adding more vias does not always increase the electromigration lifetime but it depends on the schematic layouts. The electromigration lifetime with multiple-vias will be prolonged, if there is a current sharing between the vias. The lifetime will not improve, if there is no current sharing. This would only reduce the early failure due to the misalignment during technology process properly. The number of vias and via configuration is less important than the reservoir area in improving the lifetime. The experiments in this study have shown that the current crowding effect in the reservoir area only slightly influences to the electromigration lifetime under low current density stress. However, this effect is very large in case of a higher current density stress (higher than 15mA/μm^2 from our experiment) and in case the via layouts are susceptible to current crowding. If design of via layouts in multilevel interconnects can avoid the occurrence of current crowding, the early failures will be reduced. The overall electromigration lifetime will be also prolonged as the current crowding is reduced. Our simulator appears to be a good tool to predict reservoir and via configuration effects on electromigration lifetime that could be used in or before the design phase to build in electromigration reliability in a quick way.

5.7 References

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CHAPTER 6

Conclusions

CONTENTS

An overview about the content of this thesis will be given in this chapter. The importance of main results included in each chapter is also underlined. Finally, next possible development of this research is mentioned as well as the challenging subject is highly recommended.

6.1 Summary

The study of interconnect reliability has a long history. The technology has advanced by miniaturization, integrating more and more transistors on a single chip. By necessity the interconnect structure has complex architectures, diverse materials and small features. Conventionally, in multilevel interconnects, the conductor lines are embedded in a dielectric matrix and the conductor lines are linked together by vias, fabricated on the silicon die that contains the active devices. Therefore, electromigration, thermomigration and thermomechanical failures are serious reliability concerns for integrated circuits. Multilevel interconnect failures due to very fast thermal cycle stress or the coupling of electromigration with fast temperature cycling or temperature gradients as well as the electromigration failure at vias are topics that are not fully understood. In this thesis, the effect of those failure mechanisms on the interconnect reliability have been investigated.

Firstly, this thesis starts with an introduction in which the different failure mechanisms related to this research are addressed. Their background and the motivation to trigger this research are also discussed.

In chapter 2, thermomechanical failure of a standard two level metallization currently used for power ICs under thermal cycling load is studied. A fast thermal cycling method has been introduced for the reliability tests. The

modelling of the failure mechanism and the reliability model is investigated to understand failure mechanism and to predict the lifetime under fast thermal cycling, respectively. The influence of interlayer dielectric materials on this failure mode is identified which points out a reliability problem of advanced ICs when the low-k interlayer dielectric materials are implemented.

Chapter 3 describes a study of the electromigration induced extrusion short-circuit failure in the multilevel interconnects. The effect of fast thermal cycling on this failure model has been verified. Simulations of thermal and electromigration stresses together with a no-cracking condition [1] are treated for a better understanding of the failure mechanism.

The effect of temperature gradients on electromigration performance is examined in Chapter 4. A special test chip, which integrates several on-chip heater elements and temperature sensors, has been used for the electromigration testing. Electromigration tests have been performed at uniform temperature and in the presence of temperature gradients for comparison. A typical application of this model is demonstrated that could be used for rapid characterization of power IC metallizations.

Finally, Chapter 5 presents a study of the electromigration failure at the vias of multilevel interconnects through simulation and experiment. Effects of reservoir area, reservoir layout and via layout have been characterized with the aim to optimize the electromigration lifetime. A comparison between simulation and experiment is done to illustrate the possible use of a 2D electromigration simulator to evaluate the electromigration reliability of multilevel interconnect layouts during the design phase in quick and cheap way. The current crowding effect, is also investigated through experiment using special test structures.

6.2 Conclusions

Conclusions to chapter 2

Fast thermal cycling method for reliability test is described. Special test chips has been used, in which the two level metallization system is integrated with a micro-chuck (using n^+-Si resistor) and a temperature sensor (using p/n diode) to generate a temperature swing and to measure the temperature respectively. Reliability tests under different conditions have been studied. Cracking of interlayer dielectric has been predicted through the results of the reliability

tests and is consistent with failure analysis. The modelling of the failure mechanism gives a qualitative understanding of the failure. The failure rate cannot be fitted with the Coffin-Manson equation for all test conditions of fast thermal cycling. A reliability model has been developed that can be used to fit reliability test results of all test conditions with fast thermal cycling. Reliability tests with fast thermal cycling have been performed on the interconnect systems in which different ILD materials (SiO_2 and Si_3N_4) have been used, showing that the use of Si_3N_4 as ILD gives a better lifetime.

Conclusions to chapter 3

Electromigration-induced extrusions, which result in a failure due to short circuit, has been investigated in detail. Electromigration tests have been performed under different conditions. The activation energy observed by using extrusion as the failure criteria is comparable with original electromigration process qualification which used resistance increase as failure criteria. The influence of fast thermal cycling on this electromigration failure model has been studied. The reduction in the electromigration lifetime depends on the cycling temperature range as well as the minimum temperature. The reduction increases with increasing the minimum temperature.

Conclusions to chapter 4

Electromigration under the presence of a temperature gradient has been studied. A special test chip has been described for this experiment. Electromigration tests have been performed at a uniform temperature and in the presence of a temperature gradient for the comparison. The experimental results have shown that the electromigration lifetimes in a temperature gradient are much shorter than that at a uniform temperature. Thermomigration induced by temperature gradients is small compared to electromigration. This work demonstrates the importance of temperature gradients as sources of flux divergence that essentially causes the shortening of the electromigration lifetime. The current exponent value extracted from Black's equation for electromigration in the presence of a temperature gradient is higher compared to that where there is none. A typical application of this model for characterization of power IC metallizations has been given.

Conclusions to chapter 5

Effects of reservoir area, reservoir layout, multiple-via, and via layout on the electromigration reliability of multilevel interconnects have been studied through simulation and experiment. Both works have shown the same conclusion that if one increases of the reservoir area and the number of vias, the electromigration lifetime is accordingly increased. However, a saturation of the lifetime increase is observed. The layouts of reservoir and vias in horizontal and vertical directions do not result in different lifetime. The experiments in this study have shown that the current crowding effect in the reservoir area only slightly influences the electromigration lifetime under low current density stress. However, this effect is very large in case of a higher current density stress (higher than $15mA/\mu m^2$ from our experimental results). If design of via layouts in multilevel interconnects can avoid the occurrence of the current crowding, the electromigration lifetime would be improved.

6.3 Recommendations

The test module as presented in chapter 2 can be equipped with more stress sensor elements. The stress sensors can be utilized by the piezoresistive effect of silicon. The strain gauge combined p-type and n-type diffusion resistor as reported in [2] can be appropriately applied. With this module, thermal stress in a plastic package can be measured during fast thermal cycling, which will be very useful for studying of the thermomechanical failure due to fast thermal cycling.

The study of electromigration-induced extrusion failure as presented in Chapter 3 should be extended for multilevel interconnects, in which low-k dielectric materials are implemented. Because low-k dielectric materials usually have low fracture resistance, they are susceptible to crack by extrusion of electromigration-induced.

Electromigration tests in the presence of a temperature gradient should be carried out with a larger number of devices to model the effect of temperature gradient on electromigration resistance in order to improve electromigration design rules.

Development of an electrothermomigration simulator that can be used to predict the lifetime of the metal line is used. The simulation results can be used for comparison with the experimental results as presented in Chapter 4.

The simulator could be a good tool to predict the reliability of metallization systems in the ICs, where a significant temperature gradient can be induced during the operation.

6.4 References

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